Question 1

To me, the least important subject(s) in the course was/were ...

Comments:

-system-level design(rtl/synthesis/etc),'16 FF'
-Top system level design info. I am a device engg in the fab, so i am pretty faraway from it. However no information is a waste.
-Test reliability-> only because that is where the focus of my daily work is. Not much new knowledge for me in those sections.
-to do analog/mixed signal test, so memories were probably the less (?) important. I thought it was the most interesting section, though.
-Packaging as i come from packaging background
-None i find all the topics/subjects interesting
-All of it was good
-Special circuits, devices, and technology
-Old NMOS design
-Packaging, process technology
-Being a test engineer, i can't really say there was a subject that did not interest me, but i would say the section about lithography(?) was a bit long.
-Process technoloy, but only because i am already an expert in that area. I understand that it was probably good for most others.
-Test/Yield, because i already knew bulk of material of exact fabrication steps, too detailed for a subject i do not use at work.
-Layout/stick diagrams. NMOS seems irrelevant due(?) to CMOS
-The packaging portion, because i already knew this. But i think all engineers need this information. I would think a little more time would be given to this section.
-Packaging and testing need to be 0,25 day instead of 0,5 day
-NMOS/outdated technologies
-Seems like less coverage of NMOS
--Design process and fabrication of transistor
-All are important to me. For me i think packaging was least important.
-I liked the balance of all the subjects. For diverse audience it was a good mix of subjects and covered a lot of the imortant stuff i wanted to learn.
_all subjects were important. Some (SOC design,test) were less important to me (due to existing knowledge) personally but of high relevance for other participants.
-Advanced design as i was not fully prepared for some of the circuits. Still interesting though!
-NMOS design was least important,i believe we can skip past this and go to CMOS. Low power most important.
-Older technologies, such as NMOS an EPROM. Should limit items.. (decades old … time is limited.(?)
-Layout(stick diagram)as i hardly do it in my work
-Packaging
-Information about older process methods like LOCOS,deposition
-Chapter 4
-VSLI,NMOS circuits
-Layout

Question 2

Which subject(s) should, in your opinion, be added to the course?

Comments:

-a little bit on analog design and layout
- I think the range of topics was complete. Wouldnt add or substract.
-none. Good overall coverage.
-overall, i thought it was very well balanced. I particularly liked the opportunities to see how a certain subject related back to industry
as a whole (memories dominate transistor production,wafer,DFT 5% increase in chip area-> 50% cost savings,etc)
-packaging. As you say, interconnects are the next challenges. We should different packaging tyerS(?) and how interconnect connect PKG to chip.
-Perhaps more emphasis on the latest trends such as FINFET,FDSOI
-A little bit more on how boolean is converted through synthesis into a netlist. Short time spent on it was great and i wanted to learn more. Boolean to CMOS a little m
-Active power isolation via logic. This is a long stretch as it can be separate course on it's own.
-Hard to believe something might have been missed.
-Computer architecture, JTAG testing, More Failure Analysis tools, VSLI and DFT techniques. Verileg and VHDL programming
-As is is fine, with more emphasis on Memory and their architecture.
-Nothing added as it is already quite comprehensive. Perhaps remove some material to futher expand on other areas.
-More about test cycle (burn-in,various probe tests)
-more basic material, especially on digital logic
-A basic circuit overview. My background position does not involve circuit diagrams.
-more actual design implementation/tools
-More unique test methods to catch outliers.
-More indepht discussion of the recent design issue and design technique.
-Post silicon validation techniques

-For the 4 day course no need to add anymore subjects.
-possible topic: simulation;product definition, product lifecycle.
-A bit more on logic circuits,design,etc. Very much enjoyed how modern the text is.
-Formal verification & validation. Emulation on FP?A's
-More FINFET,advanced technologies
-At the end of the day we need to understand the bottom line. So some cost info (there is little here) such as GM%, ASP etc may help understand why we are in need of doing a "smarter" design.
-More info on FINFET and industry trend on FINFET
-More details on FINFETS, more time on modern process issues
-Circuit design, memory testing
-Manufacture of MOS devices
-More background on tools used
-A36

Question 3

The level of the course combined well with my foreknowledge of this subject (1 = too easy, 10 = too difficult).

1	2	3	4	5	6	7	8	9	10	
		3		13	7	6	9	1		39
0	0	9	0	65	42	42	72	9	0	239
										6,13

Comments:
-More emphasis on FINFET, 16FF is a major node shared across all business.EDS is an emerging (and very broad) topic that could be added-> covers many discipline
-The course was a refresher from college VLSI class. So it was easy to follow along
-the course was well put together. Maybe focus more on a couple or three area's and give more detailed information would be helpful.
But if this course were spread over 5 days that would make it much better.
-overall very good. Lots of basics on many areas.
- I found the layouting questions to be difficult. I need to fresh up on some of the stuff i thought i knew.
-helped me with FEOL and BEOL (?)
-Was very good course. Was finished but wanted it to keep going.
-A very good balance
-Some areas for me were outside of my job scope so this course was an eye-opener for me.
-The first 2 days were easy because that is my area of expertise.
-Too dense for 4 days.
-No design background, so some subjects were hard to comprehend.
-for any material related to circuit operation, i had trouble following the explanation(understanding)
-A lot of material
-Semiconductor physics/ fab background
-Challanging but appropriate
-I have a EE background but not used most of the subjects on my daily job. It was difficult the first time at school but given time,
it would sink in and make sense. But not much time in 4 day class and so it was difficult.
-Varied widely. I found transistor fundamentals layout,manufacturing,circuit design challanging (as expected) others not so much
-Background is process w/some EE so this course did a fantastic job filling in holes of my knowledge.
-There wasn't enough depth in any of the topics to be considered difficult
-Some was new,much was review..but helpful to review
-Very good explaining things that i heard of but weren't so clear. The new subjects introduced in my point of view,needed a little more explanation.
-depends-> with my background , last day fits very well, already pretty well informed. Difficult time refreshing on days 1-2
-Chip qualification optoelectronics
-All are very important as course explains every angle
- I had heard of many of the topics but was never fully introduced to them so it was good to get more depth on these topics.

Question 4: The course was: too short ... too long (1 = too short, 10 = too long).

1	2	3	4	5	6	7	8	9	10	
1	4	5	6	5	9	4	2	1	2	39
1	8	15	24	25	54	28	16	9	20	200
										5,13

Comments:
-Obviously not all subjects could be covered in sufficient details, but what was covered was generally very good. I could help
with some of the details W/CMOS ESD Design (0,5 latchup protection) For example, in LV CHOS we never use a diode alone in reverse breakdown,
but rather NPN (OR PNP)
- It would have been better if the material was spaced out over 1 more day

-I think the course was not too long, but the days were long because of only 4 days. An extra day would really help.
-Definately could be 1 more day to lessen the daily download of info. Maybe even just 0,5 extra day.
-I felt it was a little short, so i'm glad that i get to keep the book for reference.
- with packaging background, it was difficult to follow design part.
-Lots of information in very short time but was relevant and very good with experienced insights
-32 hours just isn't enough, but you did well to cover what was possible.
-One more day would have been the right amount of time for such deep information.
-Could go through some of the background a bit more quickly
-Not fault of instructor, too compressed for such materials. Better to choose only certain subjects or specific backgrounds
- a lot of material for just 4 days
- Extremely condensed time.
-Too long days
-4 days is nog enough time to cover all subjects
-Just right for subjects covered through long day and homework were a challenge.
-Just right. Needed 4 days to cover all subjects.
-2 weeks would be about appropriate but it was a great overview in the four days allocated.
-the course had enough time to give an overview of the material. If used as a refresher it is the correct length.
-Maybe a catered lunch, can cut off at least 30min a day
-this is understandable
-Pretty long, would be good if spreaded out.
-5 day course would be better
-Only too short, NXP force it down to 4 days.
-some more basic to level calculations in beginning will be helpful
-Would heve been nice to dive deeper in some topics over a longer time frame

Question 5: Course was well-supported by the textbook (1 = fully disagreed, 10 = fully agreed).

1	2	3	4	5	6	7	8	9	10	
						1	6	9	23	39
0	0	0	0	0	0	7	48	81	230	366
										9,38

Comments:
-acces to the presentation material would also help
-I would have liked to have copies of the slides as well. Some of the bulletpoint were hard to find back in the textbook.
-if can have access to slides, it will refresh memory :-)
-Great book. Attention to detail is fantastic. Even covers topics that can't be easily found or researched online.
-Agree. Tekst book offers a great deal of explanation coupled with demo's and examples.
-Easy to follow in the book.
-Instructor input slides explained better than book on some topics.
-Material went along with book
-Sometimes chapters presented in different order than book.
-Excellent textbook and loved how you covered material in class so that using it as a reference in the future would make more sense.
Thank you for the book and the great illustrations!
-Textbook will serve well as reference material for topics outside my immediate expertise.
-Tekst book followed along nicely.
-the textbook is well grunded in topics that were covered along the course.
-excellent book!
-very convenient to be able to reference the book when needed. Necessary information was easy to find

Question 6: The various subjects were well-presented (1 = fully disagreed, 10 = fully agreed).

1	2	3	4	5	6	7	8	9	10	
0	0	0	0	0	2	2	9	11	15	39
0	0	0	0	0	12	14	72	99	150	347
										8,90

Comments:
-yes. Slides were arrange with flow of course.
-Brilliant explanations throughout!
-Maybe less old technology like NMOS but some history is good to understand where we were and where we are going.
-Dr Veendrick is a great presenter with a wealth of knowledge that makes him able to get his point across very easy.
-Some areas could use a bit more updating.
-Would have liked more in-depth test and less lithography (IDDQ,VLV were good)

-Some subjects could be extended, but this depends on the background of the entire class.
-I would have liked more discussion on circuit design, as i will need to read the book more, but this probably was your point.
-Some subjects(testability/DFM) were presented too quickly for any real understanding.
-Agreed though i understood not having enough time to cover packaging and FA
-Great overview of many subjects in short timespan.
-Textbook is simply a more detailed version of the course.
-There were many experience based stories to go along with the material and many visual aids
-Due to lack of time, the topics i was interested in were given a quick touch but this is understandable as the course lasted only 4 days
-I am a bit weak on layout!
-The analogies helped a lot and make things easier to visualise.

Question 7: Pleasant way of learning during the course (1 = fully disagreed, 10 = fully agreed).

1	2	3	4	5	6	7	8	9	10	
				2		3	6	11	17	39
0	0	0	0	10	0	21	48	99	170	348
										8,92

Comments:
- Towards the end of the day it got harder to be attentive
-coffee break with coffe would have been great.
-Some topics were covered very quickly but not presenters fault. Great info all packed in.
-Subjects wer explained well
-Great presentation by Dr Veendrick. Really enjoyed this course.
-Very nice disposition of the teacher, and nice laid back attitude.
-4 days a little too short, with work still going it was stressful
-Great instructor with very knowledgeable background.
-Later in days it becomes hard to focus/retain for such a long lecture
Thanks for the humor.
-Good mix of high expectations of students so we pay attention and the humor to … things right (?)
-Very engaging presentation style.
-Very pleasant! Perhaps a bit more bare bones at some points, but great overall.
-It could have been more interactive. Have more breaks to complete problems individually
-Teacher was engaging, used humor to liven up boring (at times) subjects
-The classroom section was very interactive and the teacher always engaged the students, but i for one needed more time.
-Great instructor, plenty of breaks
-Enjoyed the fun video's, good way to end the days.
-Contribution of slides with paper examples was good. Happy we reviewed the homework to verify and correct any problems.

Question 8: Good working climate in this group (1 = fully disagreed, 10 = fully agreed).

1	2	3	4	5	6	7	8	9	10	
				2		1	6	11	19	39
0	0	0	0	10	0	7	48	99	190	354
										9,08

Comments:
-Everything was extremely well organized and geared well towards learning lots in time available.
-Class atmosphere was great
-no problems
-respectful, interested audience/teacher
-very diverse group of engineers.
-Strongly agree
-Met a few bright engineers
-The variety of backgrounds made the questions interesting and helped shine a light on what different concerns people have

Question 9: Personal expectations of this course have been achieved (1 = not at all, 10 = fully).

1	2	3	4	5	6	7	8	9	10	
				1		5	11	9	13	39
0	0	0	0	5	0	35	88	81	130	339
										8,69

Comments:
-I came into the course expecting more on the technology side of the semiconductor industry (process integration)
But the course seemed a little heavy on the design side particularly digital. But i did learn quite a few new things and

how my role in the industry ties into the overall scheme of thing
-next project is in FINFET technology which i now have basics on. But like to know more details on it.
-I should have prepared for the course.
-More achieved than i ever expected! Great course.
-I've learned a lot from this course to allow to understand a lot more about each process of IC design/fabrication and have a better idea of what people from other disciplines talk about during project meetings.
-Would like to go deeper on some, but i have the book to reference.
-Agree. Was able to get the well rounded knowledge offered in this class.
-Was hoping for a bit more in-depth on some subjects, but i understand the limitations.
-Some things I didn't care about, but what i was looking for, i found.
-I know a lot more about fields other than my current job.
-More circuits schematics than anticipated.
-Would have liked a better design understanding on how a chip is designed from start to finish.
-Filled in a lot of holes, i think overall may have been better in more time.
-Provided nice refreshner and intro to topics outside my discipline.
-good review of circuit logic, device pusstes (??) was hoping for more on advanced process techn. (FINFET,etc)
-Yes to some extend, due to my previous answers.
-almost
-Would have ideally liked more time on FINFET issues
-Better understanding of how the full semiconductor process works.Gained more knowledge on new technologies and the general trends.

Question 10: This course puts my job in a better perspective (1 = fully disagreed, 10 = fully agreed).

1	2	3	4	5	6	7	8	9	10	
				1	2	2	7	9	18	39
0	0	0	0	5	12	14	56	81	180	348
										8,92

Comments:
-absolutely well worth the 4 days and a couple of late nights :-)
-Covered some topics I know well but also filled lots of blanks. Was well worth time in class. Would like to have Harry back for 1 day for failure analysis team.
-I definitely have a better understanding of the disciplines outside of my own areas.
-This course connected a lot of dots for me.
--Course filled in a lot of missing subject matter from over the years. Also, i have had no exposure to memory so i found that interesting.
-More understanding of all the respons (?) due to HW bugs
-Ties all the pieces together!
-This is to be seen
-That s for sure. Great refresher course.
-Already attended in a meeting where i was able to apply what i had learned and gave me better insight in topics discussed.

Question 11: How likely is it that you would recommend the course to others?

1 - 4 (very unlikely) 5 - 6 (unlikely) 7 - 8 (likely) 9 - 10 (very likely)

2,5		5,5		7,5		9,5				
0		0		14		25				39
0		0		105		237,5				342,5
										8,78

-For packaging the course helps indirectly.
-Great course
-Will recommend but will warn how intense and difficult it will be. Be prepared!
-Great course
- Again, would have personally liked more on advanced technology, much less on older topics (NMOS)
-All engineers should consider this as refresher sort of class, no matter the area he/she works