Three-day course: Nanometer CMOS ICs

General info

*** This course starts 8.30 and ends about 18.30 (sometimes even 18.00). It includes a few exercises during the day, but no final examination. At the end of the course, the participants will get an official certificate.

*** This course is meant as a comprehensive tutorial on selected subjects of state-of-the-art CMOS ICs for engineers working in R&D centres of semiconductor lithography and fabrication houses (e.g. ASML, Applied Materials, TSMC, Global Foundries, Samsung, Micron technology, etc.).

*** The **objectives** of this course are:

1) To get familiar with the most frequently used semiconductor terminology
2) To provide the basic knowledge and understanding of the complete development process of a chip
3) The course will enable the participants to better communicate with their technical colleagues in the field and with suppliers and customers.
4) It will place the participants' own job in a much better perspective and it will broaden their horizons.
5) Eventually, it will support the participants' motivation, as they can better understand and identify their own contribution to the total chip development process.

Contents

Introduction
The electronics (r)evolution. What is a chip. Basic concepts, definitions and terminology
Introductory overview of the development of a chip: from design to application

Wafers and transistors
substrates, wafers, basic transistor operation, CMOS

Lithography
Complete overview of state-of-the-art lithography topics and tools (incl. multi patterning, EUV, etc.), all in relation with design and CMOS process

Fabrication
Gradual introduction into the various layers and process steps from which a chip is built: from a basic 5 mask 1970 process, up to an advanced 12nm FinFET process

Memories
Memory types, basic architecture of the most important memories and memory cells: SRAMs, DRAMS, EPROMs, EEPROMS and flash memories, with a focus on multi-level and multi-layer 3-D memories.

Design

Basic understanding of transistor layout, basic design methods, libraries and library cells, design complexity in relation with lithography and process issues

Testing, yield, failure analysis

Basic chip tests. Test complexity. Yield and yield model. Random and systematic yield loss. Design for manufacturability and relation with lithography.

Packaging

Physical, electrical and thermal characteristics of packages. Influence of package on system size. 3-D packages.

What's next?

Roadblocks for further scaling. End of Moore's law. Time to market and cost (design, litho and fab cost). Combining microelectronics with micro and nano and bio-technology (MEMS, Bio-chips, etc.) to create real systems on a chip.

The course includes a copy of 2 books: "Nanometer CMOS ICs; 2017 edition" and: "Bits on Chips; 2017 edition"