Four-day course: Nanometer CMOS ICs

General info

*** This course starts 8.30 and ends about 17.30 (sometimes even 18.00). It includes a few exercises during the day and in the evening. At the end of the course, the participants can get an official certificate.

*** This course is targeted at system and IC designers, CMOS process engineers, engineers active in IC simulation, verification, test, reliability, design methods, engineers working in electronic product development and all others who need a thorough understanding of the complete development chain of CMOS Integrated Circuits and products

*** The **objectives** of this course are:

1) To understand the full design development cycle: from basic transistor and individual (library) cell layouts to complete systems on a chip
2) To acquire detailed technical knowledge on physics and fabrication of CMOS integrated circuits
3) It will enable designers and product engineers to understand all physical issues related to achieve optimum design performance
4) To achieve all knowledge for low-power chip operation incl. robustness and reliability
5) It will place the participants' own job in a much better perspective and it will broaden their horizons.

Contents

Basic principles
Basic CMOS: physics, operation and characteristics. Transistor current expressions. Capacitances

Geometry effects
Temperature behaviour. Short-channel effects, Subthreshold behaviour and other leakage current mechanisms.

CMOS technology
Summary of advanced lithography tools. Basic CMOS processing steps. Process cross sections from a basic nMOS process through an advanced planar CMOS process toward a 10 nm FinFET process.

CMOS design
Complete overview of electrical, logic, library and layout design. Some analog and mixed-signal issues

CMOS memories
Discussion on all memory architectures and properties: SRAM, DRAM, ROM, PROM, E(E)PROM, NAND- and NOR-flash memories, stand-alone and embedded memories.

VLSI and ASICs

Design flow. Hierarchy levels. IP cores. Re-use. Standard-cell design, ASICs. Design example of a signal processor from sytem level to layout level

Low-power and power reduction techniques

Battery overview. Overview of standby and leakage power sources. Summary of all existing technology options to reduce active and leakage power. Complete overview of design options to achieve minimum active power (switching or operating power) and minimum standby power (or leakage power).

Robustness of ICs

Reliability and signal integrity issues. Latch-up, Punch-through, ESD protection circuits. Hot-carrier degradation. Electromigration. NBTI. Supply and substrate noise, power integrity, on-chip decoupling, cross-talk, noise margins, EMI, EMC, soft-errors and variability, etc.

Testing, debugging, failure analysis and yield, packaging

Complete overview of existing IC tests, DfT and BIST. Basics of yield and simple yield model. Packaging characteristics and trends. Diagnostics and state-of-the-art failure analysis techniques. Repair, focused ion beam (FIB), etc.

Scaling trends and roadblocks

Scaling towards 10 nm technologies and beyond. Speed and power trends. Design, masks and processing costs. Roadblocks and solutions. End of Moore's Law!

Finally, the course includes many practical examples, problems and pitfalls of integrated circuits and comes with exercises during the day time and evenings!
On request, the course can be completed with a final examination and a certificate for those who pass.

The course includes a copy of the book: "Nanometer CMOS ICs; edition 2017"