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Electromagnetic effects have been known to affect operation of electronic circuits for several years now. The effects can broadly be distinguished into two categories: those due to Electrostatic Discharge (ESD) and those due to Electromagnetic Interference (EMI).

Electrostatic Discharge or ESD events can potentially cause physical destruction of electronic equipment. The origin of an ESD event lies in the transfer of static charge between two bodies at different electrostatic potentials. CMOS devices are vulnerable to the high potentials that get built up prior to such an event and must be adequately protected against damage.

Electromagnetic Interference (EMI) on the other hand while not physically destructive to the circuitry, prevents correct circuit operation especially when analog and RF circuit components that are part of a design are in close proximity to digital blocks that are switching at high speed.

The effects due to ESD and EMI have been exacerbated with the shrinking transistor geometries,the demand for greater integration and speed. The methodology that is applied to assess and mitigate the effects of ESD and EMI is called Electromagnetic Compatibility (EMC). EMC then employs various techniques to mitigate the negative effects due to electrostatic and electromagnetic events. The Human Body Model (HBM), Charged Device Model (CDM) and Machine Model (MM) are standards used to evaluate ESD susceptibility[5][8][18].

The next sections of this paper deals with each of these topics in detail.

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ESD is the phenomenon of a sudden transfer of charge between two bodies at different electrostatic potential. The build of charge is a well known electrostatic phenomenon and electronic equipment is always in potential danger from the high electrostatic potentials that can be achieved in such an event. For example the human body can accumulate charge with an electrostatic potential reaching about 25KV[5].

2.1 Causes of ESD and Stages of an ESD Event

The two biggest contributors of charge that constitute an ESD event, in the context of electronic devices are humans and equipment. That said, an ESD event is composed of four distinct stages [5]:

a) *Charge Generation* where static charge is transferred between bodies. There are three mechanisms which can come into play: Triboelectricity where charge transfer occurs when two differently charged bodies rub against each other, for example when a person walks barefoot across a carpet ; inductive charge generation, used extensively in inductive battery chargers, occurs when bodies in close proximity cause a transfer of charge from the charged body to the conducting body and conductive charge generation where two bodies come into contact momentarily and a transfer of charge occurs to equalize their relative potentials like that which occurs when the object being tested is handled by the automated tester handler.

b) *Charge Transfer*: The charged body comes into contact with the device or equipment and in the process of attaining an equal potential, charge is transferred from the object at a higher potential to that at the lower potential.

c) *Device Response*: At this stage the charge begins to

redistribute in the victim resulting in induced currents and voltages. Analysis determines whether the device can survive the event or not.

d) *Device Failure*: At the end of the event failure assessment, if any, can be carried out and the severity determined. Three distinct classes of failures can be seen: Hard Failures where the victim is physically destroyed; Soft Failures where the victim exhibits abnormal behavior for a short while and Latent Failures which are failures that do not get detected during assessment, but show up later.

2.2 Protection against ESD

Considering protection of the circuit against an ESD event first, we can model the necessary protection knowing the device susceptibilities. There are two main failures that can occur: the gate oxide may breakdown if the ESD event generates a potential that is high enough; and current flow near the surface of the substrate leading to heating [6][8]. The nanometer regime introduces other problems to deal with in the event of an ESD. The use of lightly doped drains (LDD) causes localized heating due to increased current densities while the presence of silicides in source/drain diffusions lead to localized current concentrations[6]. Also, special measures like coupling through antiparallel diodes [8] or a dedicated ESD Bus [4], need to be taken in order to ensure the multiple independent power supplies present in a design are not affected.

Figure 1. shows the basic protection scheme concept of using a shunt device to channel bulk of the discharge current to the power planes.

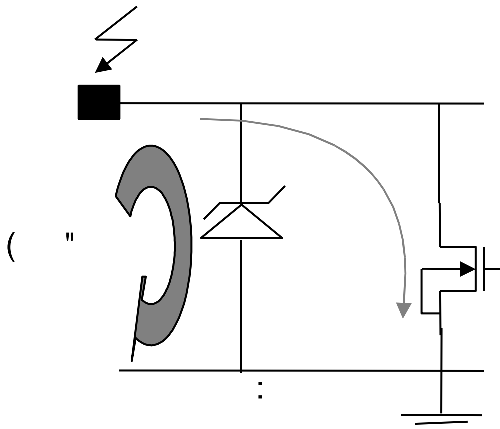

Figure 1: Protection conce)t of using a s(unt device to c(anne& t(e disc(arge current

Traditional protection schemes relied on clamping diodes to shunt the discharge current [4][8]. With thinner gate oxides and shallower source drain diffusions, more sophisticated methods of protection using grounded gate NFET devices (ggNFET) or Silicon Controlled Rectifiers (SCR's) [8] are employed to combat problems like early triggering and uneven current flow or to deal with multiple power domains. Stacked diode schemes can still be used for designs without low power implications.

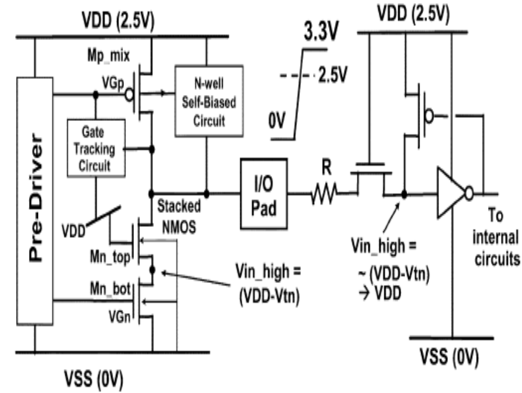

Figure 2: ESD Protection using stac ed ! " #S and !$ %e&& se&f biased P " #S

Figures 2 depicts such a scheme [4], but the working details are beyond the scope of this paper. However, it should be mentioned here that a number of these devices operate in the snap back mode i.e. at a certain critical current density a bipolar device is triggered in the substrate to bring the IV characteristic into the ESD holding window from the trigger window. Figures 3 and 4 depict this phenomenon [8].

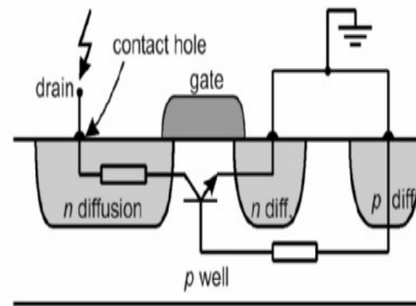

Figure ': Device %it(buried bi)o&ar device and ba&&asting resistance for sna)bac mode o)eration

In the specific case of I/O's the issue of impedance matching does not pose problems since , even if we assume tunable impedances they become part of the core logic and ESD protection can be designed taking them into account.

Lastly, humans can contribute greatly against ESD

by following simple guidelines like treating all equipment as ESD sensitive and wearing grounding wrist straps or foot straps.

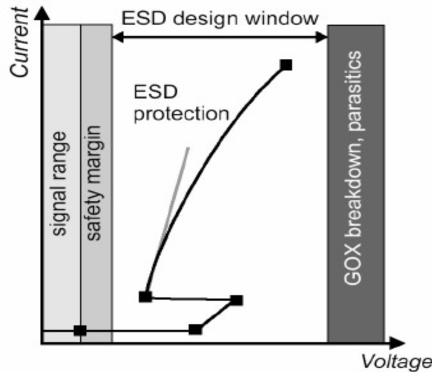

Figure *: Triggering and (olding %indo% in Sna)bac mode

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Traditionally, ESD characterization has been through direct measurement. This is however a destructive process. Recent advances have made it possible to combine process and design simulation under ESD conditions. This is however computationally intensive. The reason for this is simply that in order to model behavior under ESD conditions the current analysis at every node proves expensive. In addition even if support for snapback and thermal effects is added to device models the simulation will be time consuming in order to model the exact behavior under ESD conditions. ESD DRC's provide a faster solution but are limited in the fact that they are not quantitative analyses and can only discover marked elements and not locate other critical devices overlooked by the designer[6][7][8].

Recent developments have made it possible to use EDA tools to assess the vulnerability to ESD, but a full analysis through simulation is still expensive and not really necessary since testing for ESD compliance on product samples is an inherently destructive process. Thus no matter how accurate the simulations are there will always be one batch of prototypes that will be destroyed when being assessed for ESD hardness.

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EMI refers to the degradation of circuit performance due to switching currents interfering with other circuits in proximity to the switching block in the presence of an electromagnetic disturbance. EMI itself may be differentiated into three kinds: conductive, magnetic field coupled and electric field coupled emissions [8].

The actual mechanism of EMI in todays' circuits is quite complex due to it's close relation to the IC assembly hierarchy. Figure 6 shows the different mechanisms of EMI that exist on a packaged system.

'.1 Causes and "ec(anisms of E "I

The different mechanisms of EMI in the DSM era is spread across the hierarchy of IC assembly. It is generally accepted that the source for EMI is dynamic switching currents on the silicon die. There are however a few coupling mechanisms that contribute to the degradation of performance. The first is the normal mode radiation due to signal path return loop and the other is the common mode excitation of the power/ground plane due to switching currents from the chip[]. Other mechanisms such as return path irregularity (caused due to say a slit in the ground plane and leading to uneven current distribution) also contribute towards electromagnetic radiation [8].

There is also a major problem with dc resonance on the power and ground plane. At frequencies greater than a few hundred megahertz the power and ground lines pair up and act as a parallel plate transmission line resonator. This has great implications for the integrity of the power supply rails and gets more problematic with multiple independent power supplies in low power designs[8].

'.2 Contro& of E "I

The most common means of minimizing radiated emissions involve the use of decoupling capacitors and good layout practices for the power supply planes and lines[1][2][3][11][12][15]. These measures are implemented at a chip level as well as the board level.

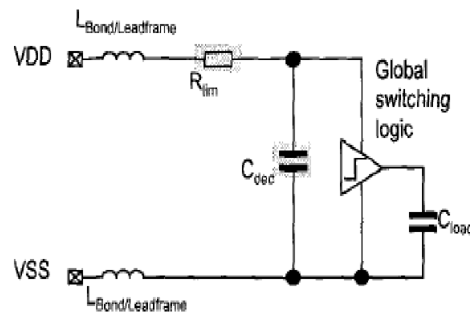

Figure +: , sing Decou)&ing ca)acitors to minimi-e E "I due to s%itc(ing currents

Figure 5 shows the concept of using decoupling capacitors where the limiting resistance and capacitance limit off chip current and provide a local recharging current respectively. On die decoupling capacitors between power and ground lines have been

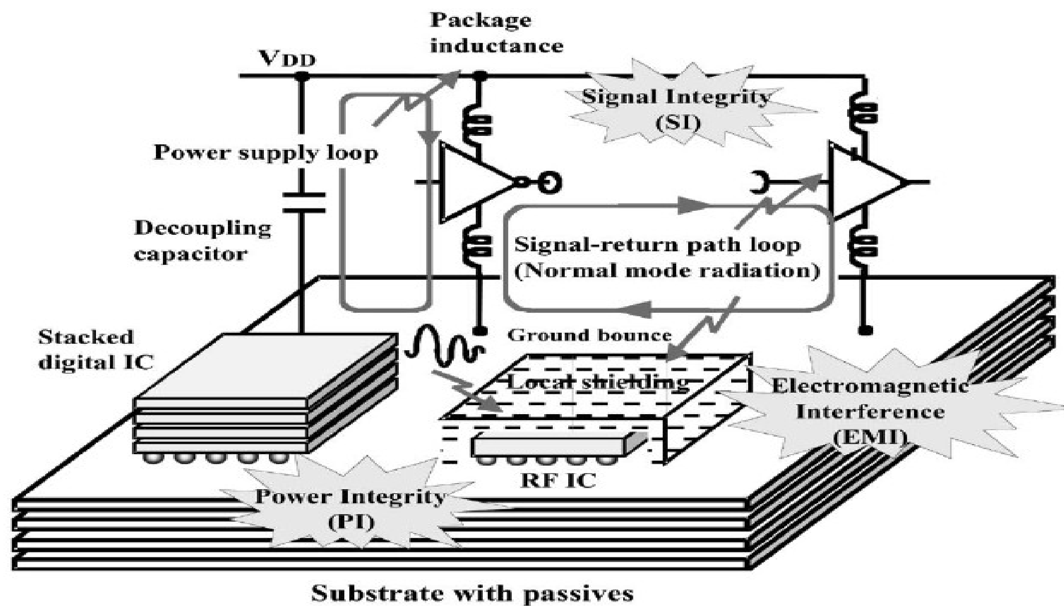

Figure .: Sources and "ec(annisms of E"I on a SoP

shown to be effective in localizing switching currents especially in isolating the short through current generated when I/O blocks switch[8]. Other measures include good board layout, bonding wire practices and shielding techniques (like Faraday cages [16]) to minimize the coupling paths. Ferrite beads may be employed to filter out high frequencies on cables[11]. On the chip die, good layout and power supply design can mitigate the effects of EMI to a great extent. It is also important to ensure clock tree design as it has the highest switching activity and consequently the greatest contribution towards EMI. Paradoxically, the performance optimization goal is towards zero clock skew, but this is not good from an EMI point of view. The solution to this problem lies in "clock smearing": the signal edges should be distributed over a time slot which should be made as long as allowed by the operating frequency and the circuit delay path. The resulting effect is comparable to a spread spectrum path meaning that high emission amplitudes at discrete frequencies decrease but other low emission amplitudes rise[2], [14].

It is important to consider impedance matching to ensure that the pads do not contribute towards EMI because of step change in the width from the trace to the via. In this case proper routing techniques and optimization of pad and anti-pad radii can help in minimizing the effects of EMI [11].

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It is no longer possible to make EMI considerations "add on" as was the case for technologies in the micrometer regime. The decreasing geometries and increasing density make electronic designs more susceptible to EMI. Most of the evaluation is carried out using the so called source-path-victim model. In order to estimate EMI a three pronged approach has been proposed: use behavioral models for switching currents in digital modules based on their BSIM models, back annotate the RLC parasitics of noise propagation paths and correlate the results from the two models through direct measurement[1][3]. While it is simple to make a qualitative analysis, analyzing dynamic currents quantitatively is computationally challenging. However, there have been advances made in FDTD methods that show promise[8]. There is also a method of using logical depth to model digital logic blocks in order to model the switching currents. Thus it is possible to estimate the EMI activity at a reasonable cost and effort.

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The advent of DSM technologies has only exacerbated the problems posed by electromagnetic disturbances on the performance of electronic circuits. It has become clear that in order to shield an electronic design from ESD and EMI events, a comprehensive methodology has to be evolved. This methodology

applied towards ensuring correct circuit operation at acceptable emission levels is termed as electromagnetic compatibility (EMC).

*.1 Conce)t of E″C

Methodology adopted to assess the designs' vulnerability to electromagnetic disturbance and the analysis and mitigation of the emissions from the design is termed as Electromagnetic Compatibility. As is already indicated, there are two aspects to EMC, namely:

a) the design does not emit unreasonable levels of emissions making it safe for use near humans.

b) the “hardness” or susceptibility of the design to external electromagnetic disturbance, determining the environment in which it is safe to operate the device

By making the distinction in the assessment it is possible to apply and ensure electromagnetic compatibility even for the complex designs today.

*.2 ″et(ods in , se to ensure E″C

Due to the scaling of device geometries, devices are more susceptible to electromagnetic disturbances today than ever before. There are also issues that arise due to the density of integration and low power issues. Thus traditional methods of ensuring electromagnetic compatibility while by no means redundant, are no longer powerful enough to meet the standards that designs have to meet today. The need to incorporate EMC into the design and development cycle is extremely important.

Traditional standards to ensure EMC are still relevant because they determine the end compatibility of the product from the two aspects of EMC detailed above. However, in order to incorporate EMC into the development cycle, methods to evaluate ESD and EMC issues must be available in EDA tools. Several tools exist that can assist designers in evaluating signal integrity and power integrity issues [20]. These tools can be adapted to allow the designers to evaluate the EMC of the device. The main classes of EDA tools that exist today to assist EMC evaluation are[9]:

a) Analytical Models : use simple closed form expressions to calculate field parameters. Usually, they are applied to pre-defined geometries with known solutions. These have the advantage of being fast and simple to use but suffer from the limitation that each expression has limited capabilities leaving the user to decide whether the expression is applicable to the situation.

b) Numerical Models: solve bounded field equations to assess the EMC. These are promising tools but are computationally intensive and so slow to run. A number of candidates using different techniques like Finite Element methods, surface integral techniques or Finite Difference Time Domain methods are applied here and each one of them is better suited for one application or the other.

c) Rule checking models: these are tools that check the geometry and are intended to help designers avoid costly mistakes early in the design cycle, rather than predict the electromagnetic behavior of a design. While they do not require the user to have prior knowledge of the electromagnetic behavior, it is essential that the user be able to identify the critical nets. Another shortcoming of this technique is that the rules are quite unique to the design meaning that the flexibility of the tool is limited.

d) Expert System Models: these relatively new techniques attempt to extract the electromagnetic behavior of a design in a manner similar to an experienced EMC engineer. They rely on design information from other tools and interactive inputs with heuristics and decision making tools in order to predict the electromagnetic behavior of a design. While this seems unreasonable, some newer tools using this technique have shown promise.

These assessment tools provide estimates of the response to electromagnetic disturbances. These will have always have to be corroborated with direct measurements. The direct testing of ESD hardness, defined by the model (HBM, MM or CDM) and for which the protection is designed, is inherently destructive and is usually limited to extensive prototype testing. EMI hardness, defined in terms of power or field strength by governing bodies like the FCC, on the other hand can be tested using inductive probes on sensitive locations[1][3][13]. It is possible to fabricate sample and hold structures on prototype devices to obtain highly accurate estimates[3]. There have also been recent improvements in near field mapping, high frequency current measurement and far field mapping making EMC a tractable problem, even for todays complex designs[8].

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The discussion above introduces the concepts of ESD and EMI and the problems they cause. EMC is introduced as a concept as well. It is clear that in order to prevent designs in the nanometer regime from being affected by electromagnetic disturbances, it is essential that EMC is considered early in the design cycle. Recent advances in the application of analytical techniques to EDA tools to assist in EMC assessment mean that the ability to ensure compliance for today's

designs is still possible. However, the methods and tools need to mature for a number of reasons; the foremost of which is the fact that compatibility assessment is still design-centric. Future work in this area will revolve around incorporating electromagnetic effects into the design phase keeping in mind that the burden on a design engineer is already high. Following the guidelines for IC and PCB design from previous generations will definitely go a long way in minimizing the effects of EMI and ESD. However, advances in the ability to predict the EMC becomes critical with nanometer transistor geometries and ever shortening design cycles. Thus, in my opinion future work will relate to “EMC Aware” tools that assist the designer in creating EM compliant designs.

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[1] T. Steinecke, M. Schmidt, H. Koehne, W. John, "EMC Modeling and Simulation on Chip Level", 2001 IEEE EMC International Symposium Record, Vol. 2,2001

[2] T. Steinecke, "Design-In for EMC on CMOS Large-Scale Integrated Circuits ", 200 1 IEEE EMC International Symposium Record, Vol. 2,2001

[3] T. Steinecke, M. Schmidt, H. Koehne, W. John, “Behavioral EM1 Models of Complex Digital VLSI Circuits”

[4] Ming-Dou Ker, Kun-Hsien Lin, “Overview on Electrostatic Discharge Protection Designs for Mixed-Voltage I/O Interfaces: Design Concept and Circuit Implementations”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 53, NO. 2, FEBRUARY 2006

[5] Matthew N. O. Sadiku and Cajetan M. Akujuobi, “Electrostatic Discharge (ESD)”, IEEE POTENTIALS, DECEMBER 2003/JANUARY 2004

[6] Nitin Mohan and Anil Kumar, “Modeling ESD Protection”, IEEE POTENTIALS, FEBRUARY/MARCH 2005

[7] Toshio Sudo, Hideki Sasaki, Norio Masuda and James L. Drewniak, “Electromagnetic Interference (EMI) of System-on-Package (SOP)”, IEEE TRANSACTIONS ON ADVANCED PACKAGING, VOL. 27, NO. 2, MAY 2004

[8] Harald Gossner, “ESD protection for the deep sub micron regime – a challenge for design methodology”,Proceedings of the 17th International Conference on VLSI Design (VLSID’04)

[9]T. Hubing, J. Drewniak, T. Van Doren, and N. Kashyap, ”An Expert System Approach to EMC Modeling”, IEEE 1996

[10] François Clément, “Formulating an EDA solution to ESI”, EE Times-Asia, November 1-15, 2007

[11] Aki Nakatani, “Reduce EMI with proper SI design”, EE Times-Asia, April 1-15, 2008

[12] Cameron Katrai and Chris Arcus, “EMI Reduction Techniques”, Pericom Application Note 11, November 2000

[13] “EMI Characteristics”,SynQor Application Note 00-08-02, December 2000

[14] Kelly Maas,”Spread spectrum clocking to reduce EMI”, EE Times-India, April 2008

[15] Shane Hudak,“EMI shielding strategies for design and attachment options”, EE Times Asia, December 2000.

[16] David Petry, “Eliminating EMI protection components”, EE Times-India, December 2007

[17] Dale Reed, “Minimizing RF effects during PCB design”, EE Times Asia, 2001

[18] Bill McCulley, “Managing EMI in Class D Audio Applications”, EE times India September 2008

[19] Ming-Dou Ker and Cheng-Cheng Yen ,“Latchup-Like Failure of Power-Rail ESD Clamp Circuits in CMOS Integrated Circuits Under System-Level ESD Test”, IEEE 2007

[20] M J Hawley and A J. Smith, ”A USERS PERSPECTNE OF EMC AND SIGNAL INTEGRI‘IY TOOLS”, IEEE 1995