Mixed-Signal Testing & DfT Techniques

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Outline

- Mixed-Signal Test Problems
- Mixed-Signal DfT Techniques
- IEEE Standard for a Mixed-Signal Test Bus
- DSP-Based Mixed-Signal Testing
- DSP-Based Mixed-Signal SoC Self-Testing

Mixed-Signal Test Problems

The Role of Testing

- The role of testing is to detect whether something went wrong.
- Diagnosis, on the other hand, tries to determine exactly what went wrong & where the process has to be altered.
- Test objectives
  - Design verification
  - Ensure product quality
  - Diagnosis & repair

What are we after?

- Design errors
- Fabrication errors (caused by human errors)
- Fabrication defects (caused by imperfect manufacturing process)
- Physical failures

Costs of Testing

- Design for testability (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Test development
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - Automatic test equipment (ATE) capital cost
  - Test center operational cost

Components of an ATE

- Powerful computer
- Powerful 32-bit Digital Signal Processor (DSP) for analog testing
- Test Program
  - written in high-level language) running on the computer
- Probe Head
  - actually touches the bare or packaged chip to perform fault detection experiments
- Probe Card or Membrane Probe
  - contains electronics to measure signals on chip pin or pad

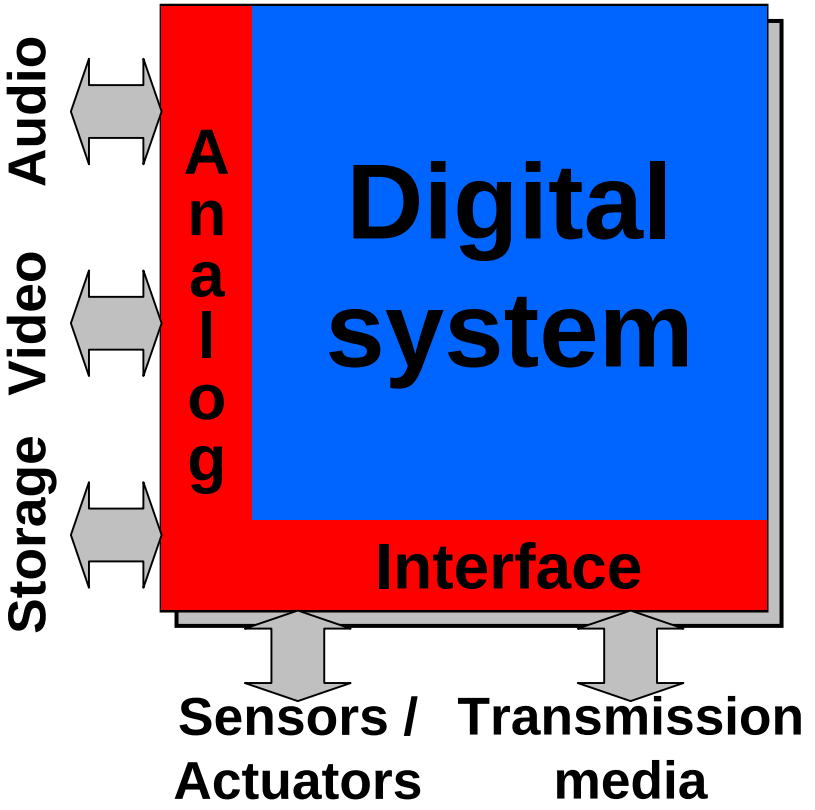
Automated Test Equipment Cost

- Tester cost = $b + \Sigma(m \times x)$
- Other cost factors
  - Tester depreciation
  - Tester maintenance cost
  - Test operation cost

Tester segments	*b*	*m*	*x*
	Base cost	Cost per pin	Pin count
	K$	$	
High-performance ASIC/MPU	250 – 400	2,700 – 6,000	512
Mixed-Signal	250 – 350	3,000 – 18,000	128 – 192
DfT Tester	100 – 350	150 – 650	512 – 2500
Low-end μC / ASIC	200 – 350	1,200 – 2,500	256 – 1,024
Commodity Memory	200+	800 – 1,000	1,024
RF	200+	~50,000	32

[ITRS 2001]

Mixed-Signal System-on-Chip



- Analog/mixed-signal circuitries are essential in real-world systems.

Mixed-Signal vs. Digital Testing

	Digital	Analog
Test signal	Single type	Multiple types
Response analysis	Direct interpretation	Need mathematical post-processing
Measurement requirement	Low-precision	High-precision
Fault model	Mainly catastrophic	Both catastrophic and parametric
Fault-free response	Binary vectors	Tolerance range in multi-dim. space

Analog/Mixed-Signal Testing Problems

- Size not a problem.
- Much harder analog device modeling
  - No widely-accepted analog fault model.
  - Infinite signal range.
  - Tolerances depend on process and measurement error.
  - Tester (ATE) introduces measurement error.
  - Digital / analog substrate coupling noise.
  - Absolute component tolerances +/- 20%, relative +/- 0.1%.
  - Multiple analog fault model mandatory.
- No unique signal flow direction.

Current Status

- Specification-based (functional) tests
  - Tractable and does not need an analog fault model.
  - Long test time.
  - Expensive ATE.
  - Long test development time: application, setup dependent.
- Structural ATPG – used for digital, just beginning to be used for analog (exists)
- Separate test for functionality and timing impossible.

The Challenges

- ATE cost problem
  - Pin inductance (expensive probing)
  - Multi-GHz frequencies
  - High pin count (1024)
- High-speed serial interfaces are gaining growing popularity.
  - High speed, differential, low voltage swing, large numbers of pin counts.
- Analog effects appear as digital clock speeds increase and reach fundamental limits.

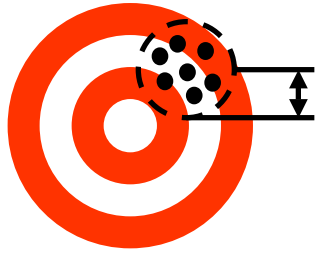
Solutions?

- Employ DfT techniques to limit the functional test performance envelope in production by
  - Reducing I/O data rate requirements,
  - Enabling low pin count testing, and
  - Reducing the dependence on expensive instruments.

- Structural testing methodoloty.

Mixed-Signal DfT Techniques

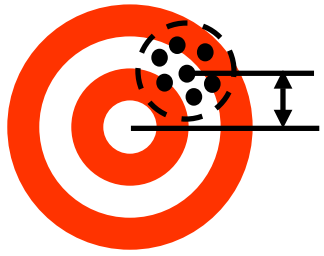
Fundamental Issue of Analog Measurement - Precision*



- Definition
  - Measurement sample deviation relative to measurement mean, e.g. standard deviation (σ_{MEAS}) of a set of measurements
- Sources of imprecision: various noise
- Basic technique to increase precision: integration
  - the more samples averaged, the better

*S. Sunter, ITC tutorial #15, 1999

Fundamental Issue of Analog Measurement - Accuracy*

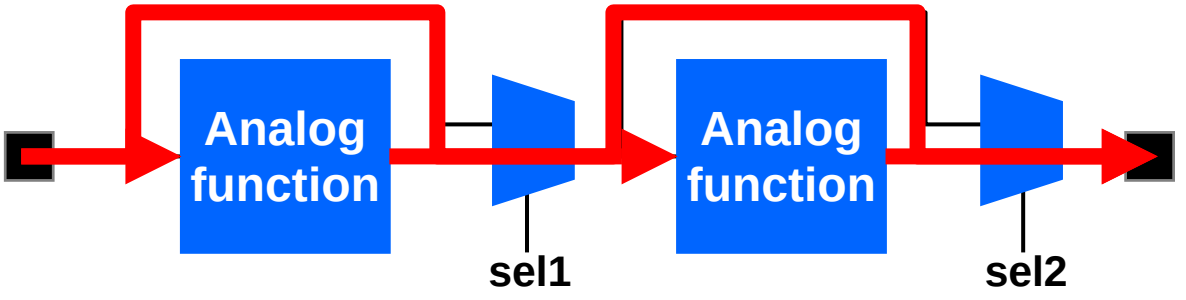


- Definition
  - Measurement mean relative to true mean, e.g. average measurement error ($\mu_{MEAS} - \mu_0$)
- Sources of inaccuracy: systematic errors
- Basic technique to increase accuracy: substraction
  - e.g. measure with/without stimulus, inverted/non-inverted

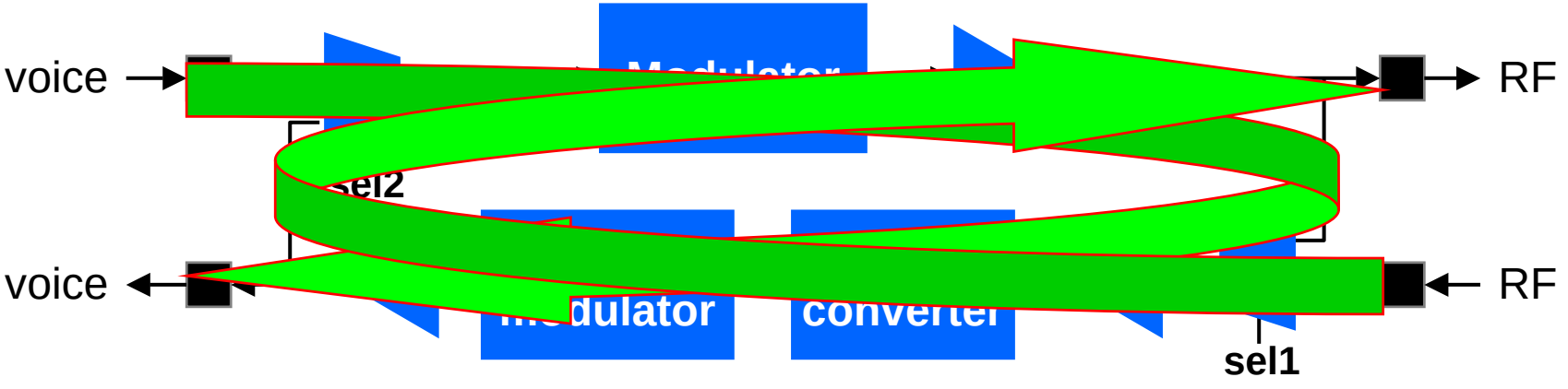
*S. Sunter, ITC tutorial #15, 1999

Reconfiguration Techniques

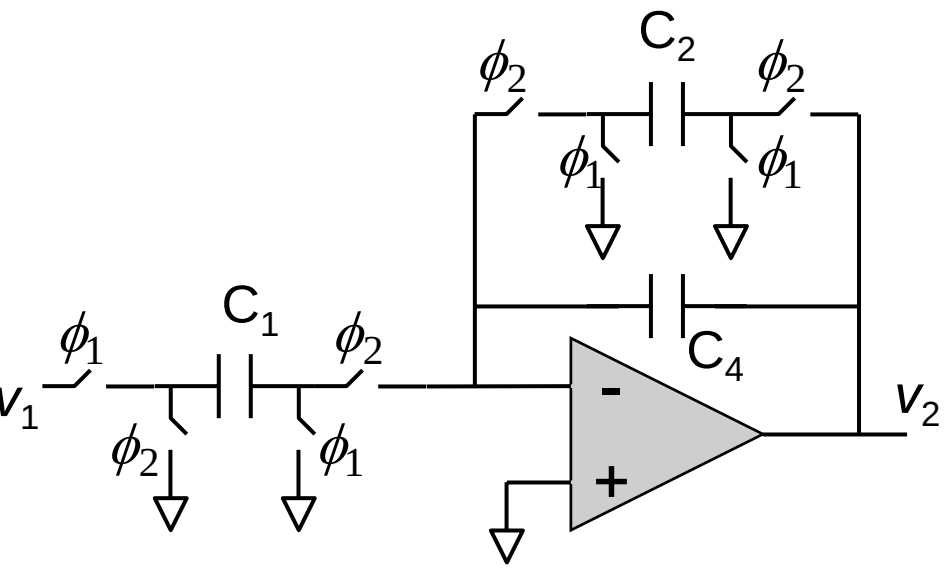
- Bypass to gain accessibility of internal nodes



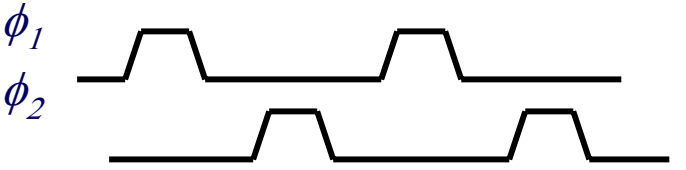
- Loop around for back-to-back testing



A DfT Technique for SC Filters [Soma VTS'94]

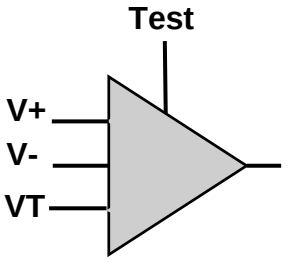


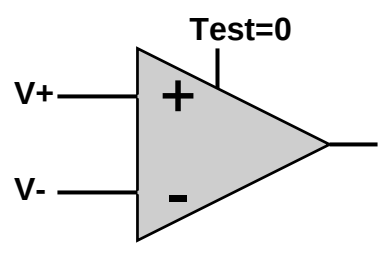
- In mission mode:

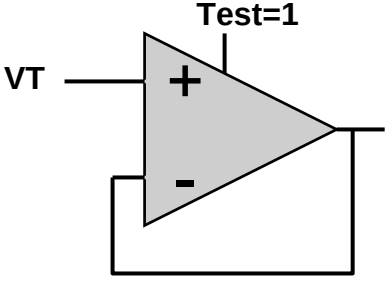


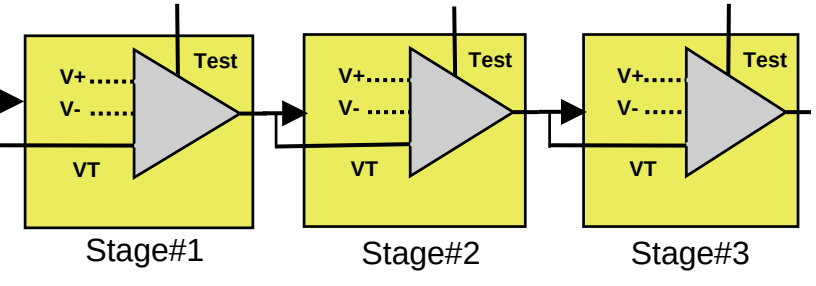
- In test mode, bypass a filter stage by converting it to an all-pass gain stage
  - Open grounding switches
  - Close signal path switches
  - $v_2 = -(C_1 / C_2 || C_4)\ v_1$
- Gated 2-phase clock signals

SW Opamp Design [*Huertas VTS'96*]



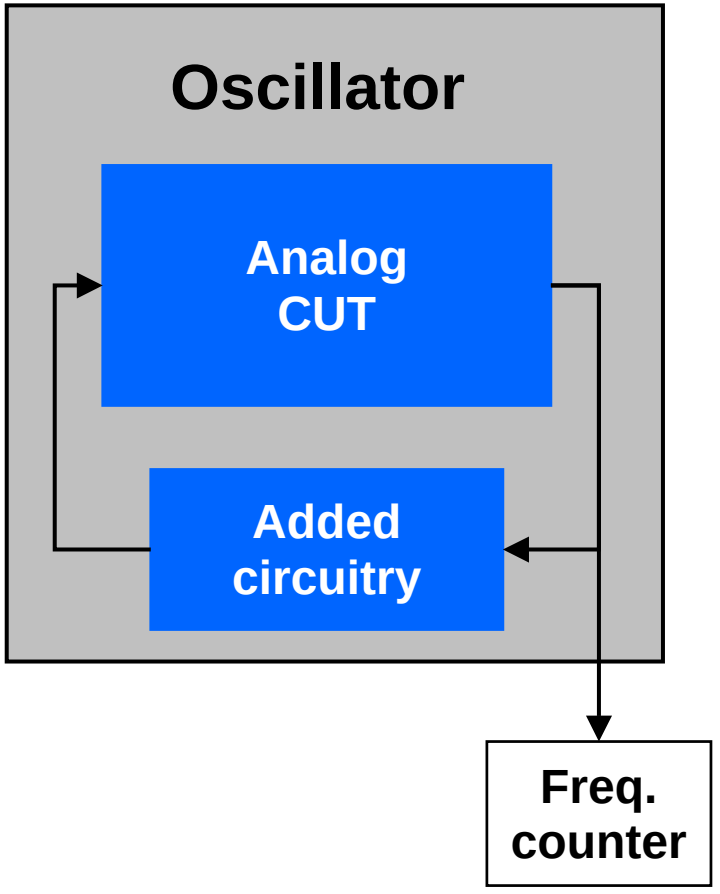






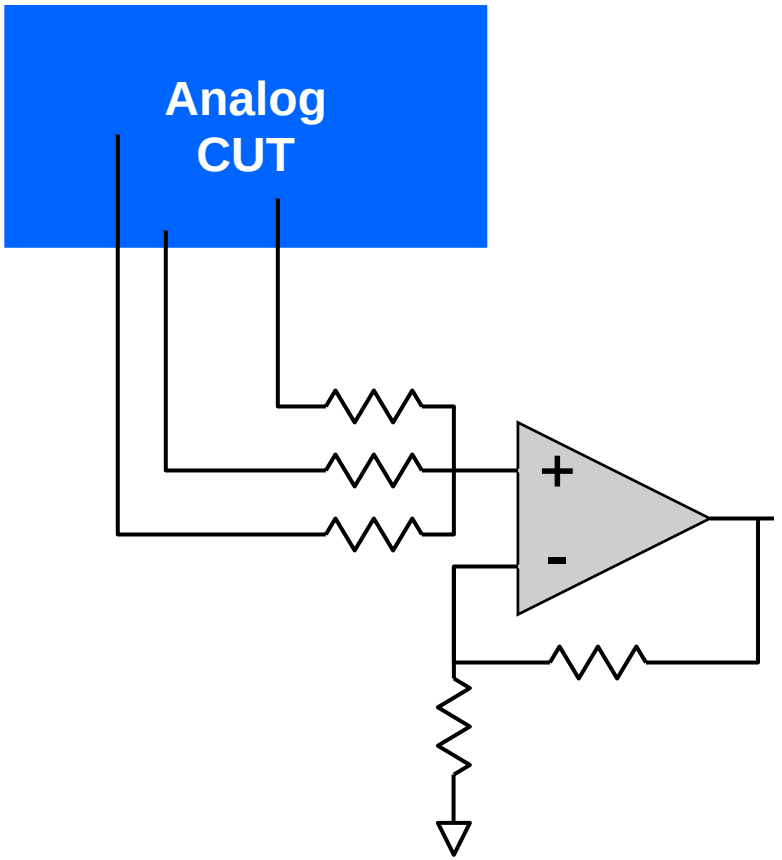
- SW opamp
  - With additional inputs: Test, VT
  - Test = 1: unit buffer
  - Test = 0: regular opamp
  - VT is connected to the output of previous stage
- In test mode
  - Test = 0 for stage under test
  - Test = 1 for others
- Switches are inserted on small signal path to reduce performance degradation

Oscillation BIST [*Kaminska VTS'96*]



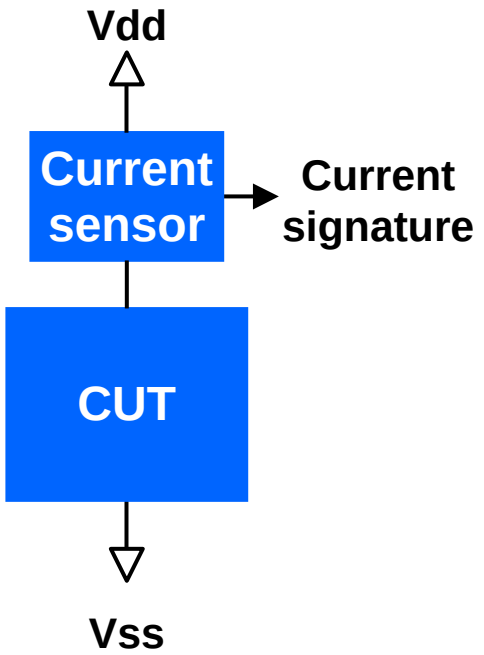
- Analog CUT plus added circuitry become an oscillator in test mode
  - Oscillation induced through positive feedback
- Defects cause deviations in
  - Oscillation frequency
  - Oscillation amplitude
- Very sensitive to process variations
  - Causes yield loss

Analog Checksum [*Chatterjee D&T'96*]



- Sum the voltages at selected internal nodes
- Fault effects appear as error voltage

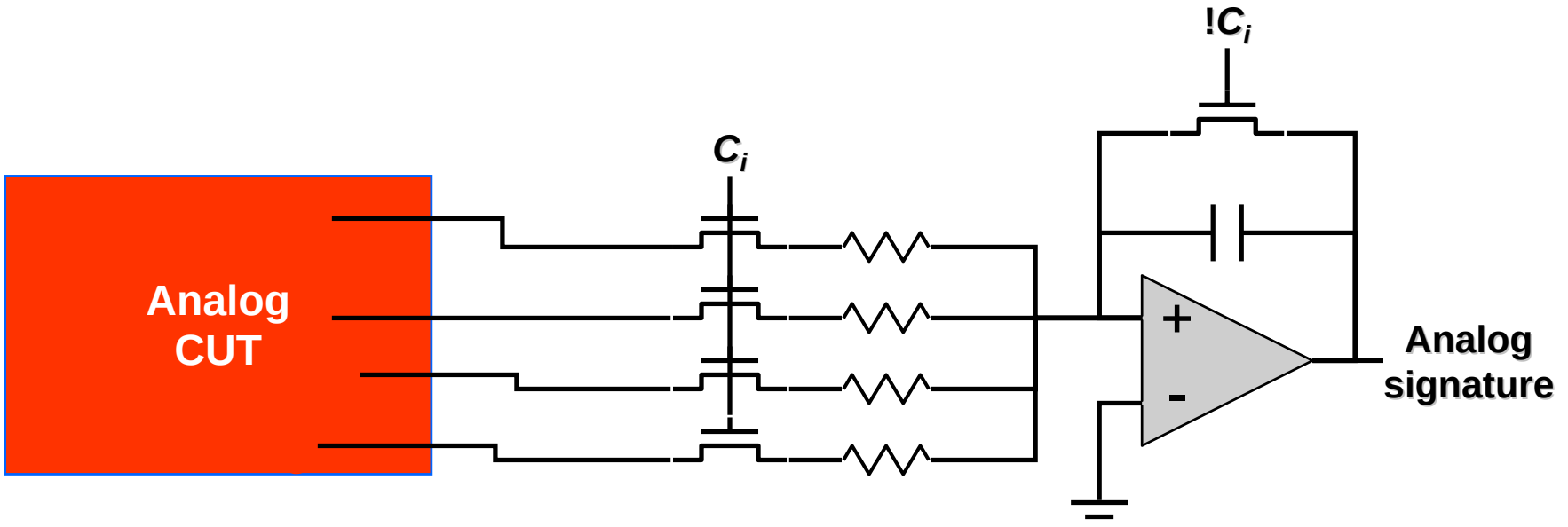
Built-in Current Sensor



- Insert current sensor between CUT and Vdd (Vss)
- Use current signature to make pass/fail decision
- Compare to:
  - DC threshold (on-chip or off-chip)
  - Expected spectrum (off-chip)
- Cons: resistance in Vdd Path

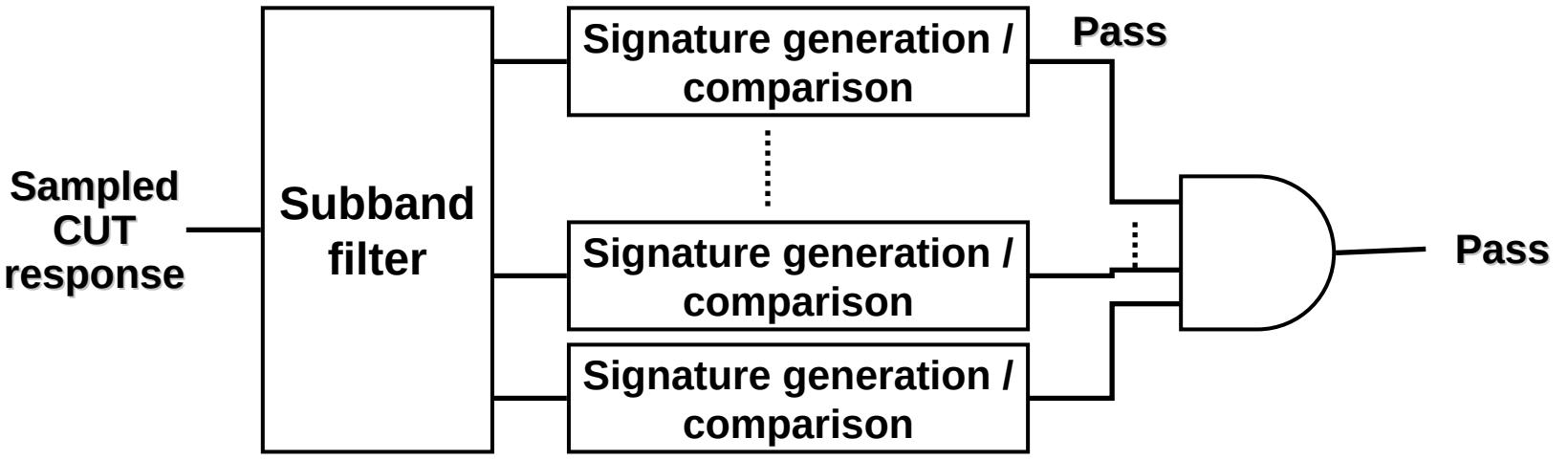
Analog Output Response Compaction

[Bertrand EDTC '97]



- Opamp-based integrator for analog signal compaction
- Suffer fault aliasing problem

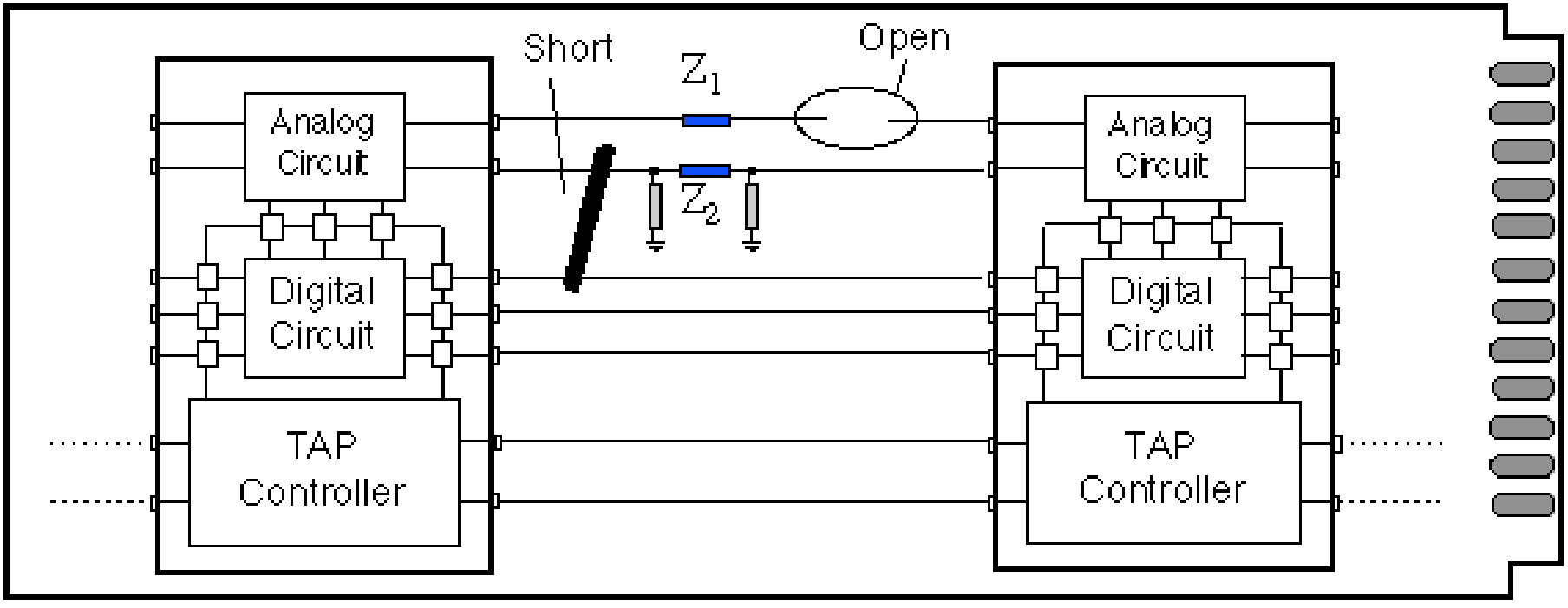
Subband Filtering [Abraham ITC'99]



- Pros
  - Subband filtering requires relatively less hardware
  - More immune from fault aliasing problems
- Cons
  - Requires on-chip ADC

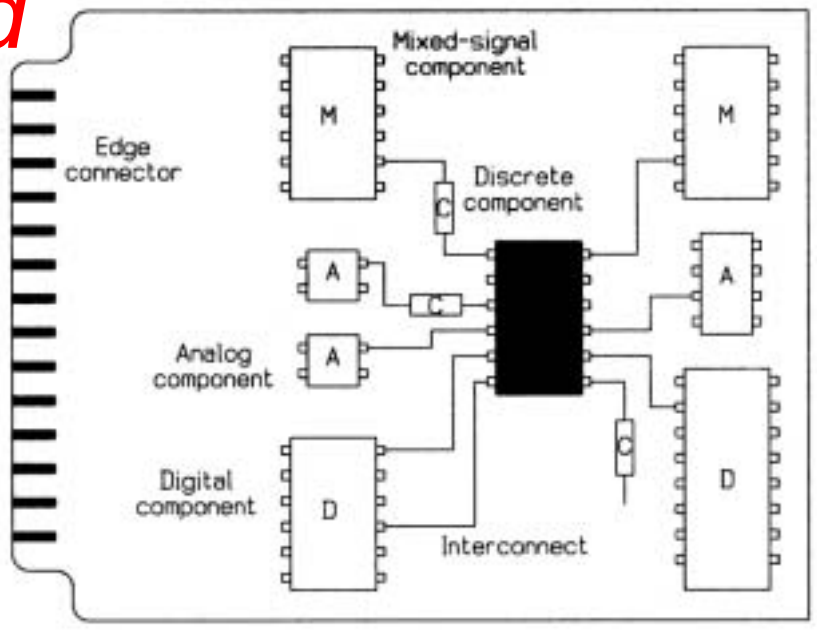
IEEE Standard for a Mixed-Signal Test Bus

Test Board with Mixed-Signal Parts



- The introduction of analog components to 1149.1 compliant chip introduces new problems.
- The ability to isolate faulty interconnects on the analog I/O pins does not exist!!

Scope of the Standard



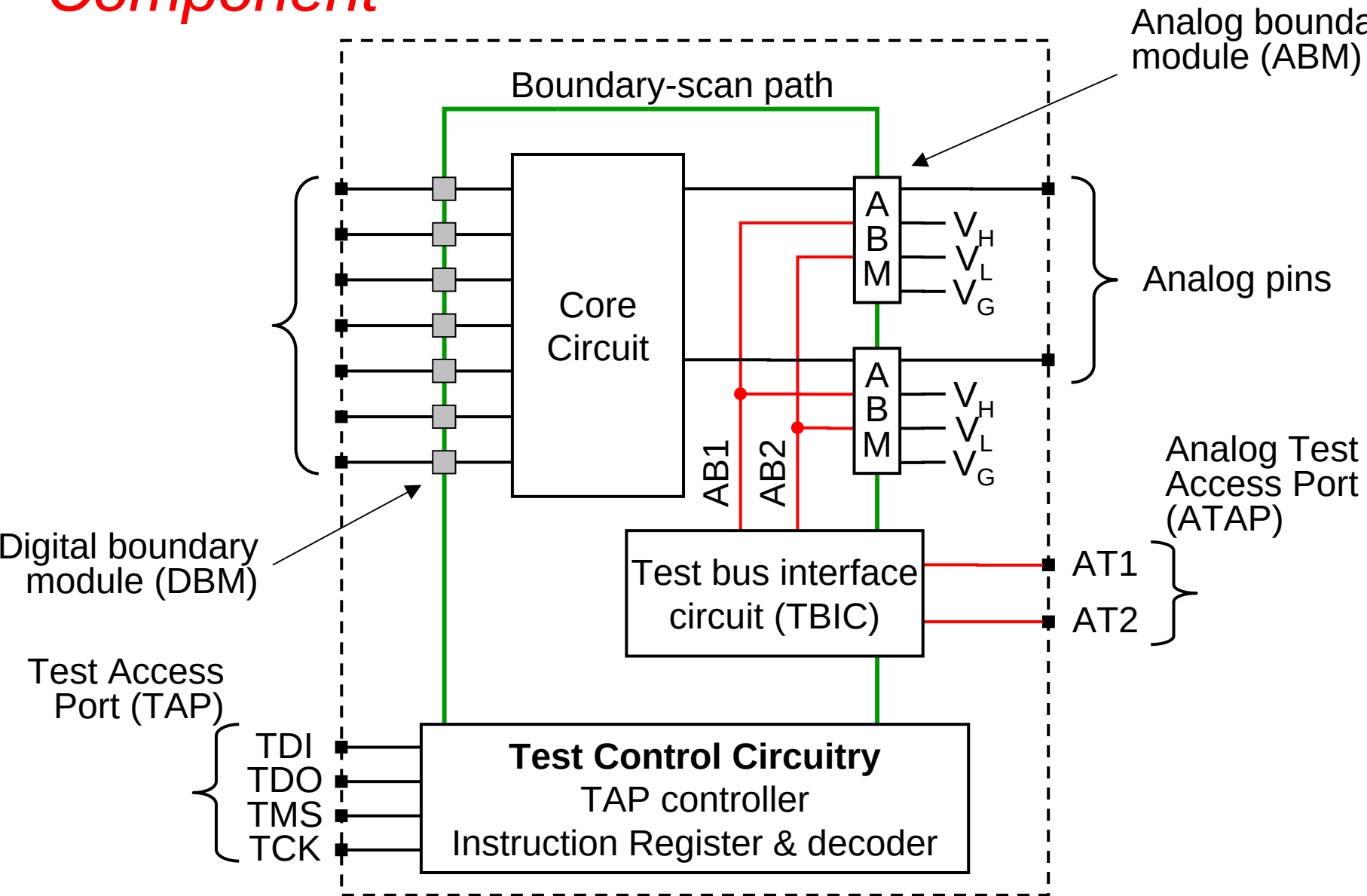
- Interconnect test
  - Testing for opens and shorts among the interconnections in a PCA (Printed Circuit Assembly).
- Parametric test
  - Making analog characterization measurements.
  - Testing for presence and value of discrete components in a PCA.
- Internal test
  - Testing the internal circuitry of the mixed-signal component itself regardless of whether it is part of a PCA.
  - Not mandatory.

Feature Overview

- Capabilities
  - Continuous-time voltage, current access via two analog pins.
  - Measure R, L, C, gain, etc. with < 1% error.
  - True differential access, and other options.
  - 1149.1 compliant

- The idea is to include a set of digitally-controllable analog boundary cells that can perform the following four functions:
  - Disconnect the I/O pin from the analog core.
  - Set the I/O pin at a logic high or low level.
  - Detect the logic level present on the I/O pin.
  - Connect the I/O pin to a two-wire analog test bus.

A Minimally Configured 1149.4-Conformant Component



Required Test Functions for Analog Pins

- Isolation
  - Connect to core.
  - Disconnected from core (CD state).
- Perform tests equivalent to 1149.1
  - Drive pin's V_{max}, V_{min} (DC).
  - Compare V_{PIN} to pin's V_{TH}.
- Facilitate analog parametric tests
  - Deliver analog ground (V_G) via power rail.
  - Deliver current to pin via AT1 pin and AB1 bus.
  - Monitor pin's voltage via AB2 bus and AT2 pin.

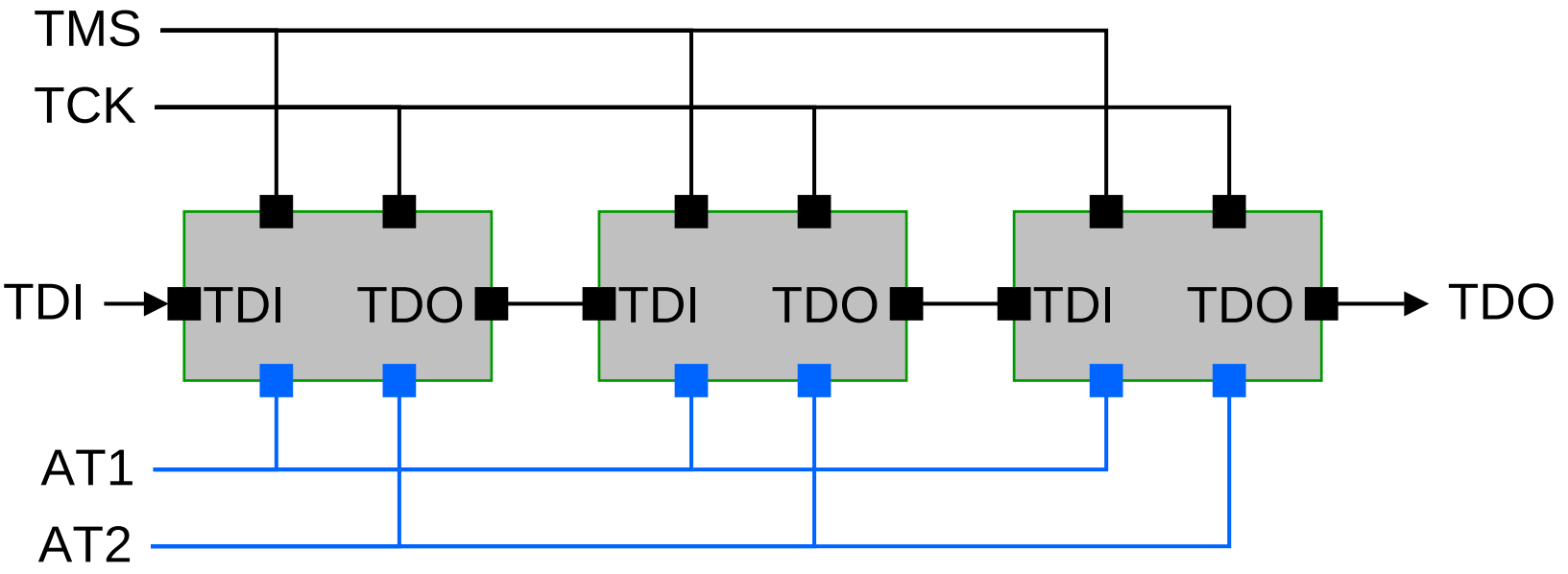
Test Access Port (TAP) Pins

- TCK – test clock
- TMS – test mode select
- TDI – test data in
  - Instruction or scan data
- TDO – test data out
  - Test results or for next chip
- TRST – optional reset

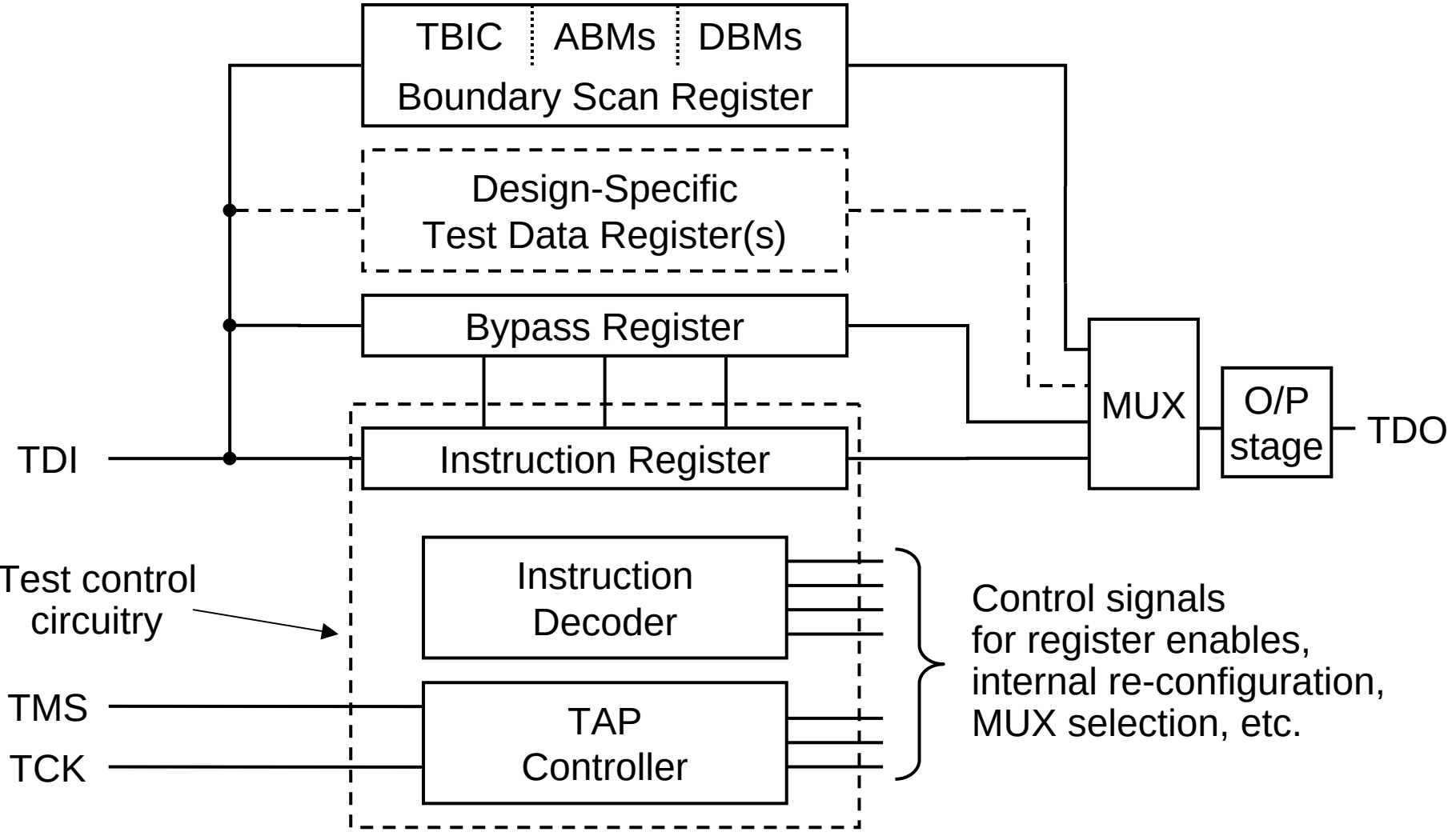
Analog TAP pins

- AT1 – stimulus current bus
  - At least capable of conveying ±100 μA
    - May be any combination of AC and DC
    - DC – 10 KHz minimum bandwidth
    - Sufficient for state-of-the-art ATE to achieve < 1% error
  - Convey response output (optional)
- AT2 – resultant voltage bus
  - At least capable of conveying ±100 mV
    - Range: (V_{SS} - 100 mV) to (V_{DD} + 100 mV)
    - Ensures that protection diodes are not partially activated.
  - Convey stimulus input (optional)
- AT1N, AT2N – inverted pins for differential testing.

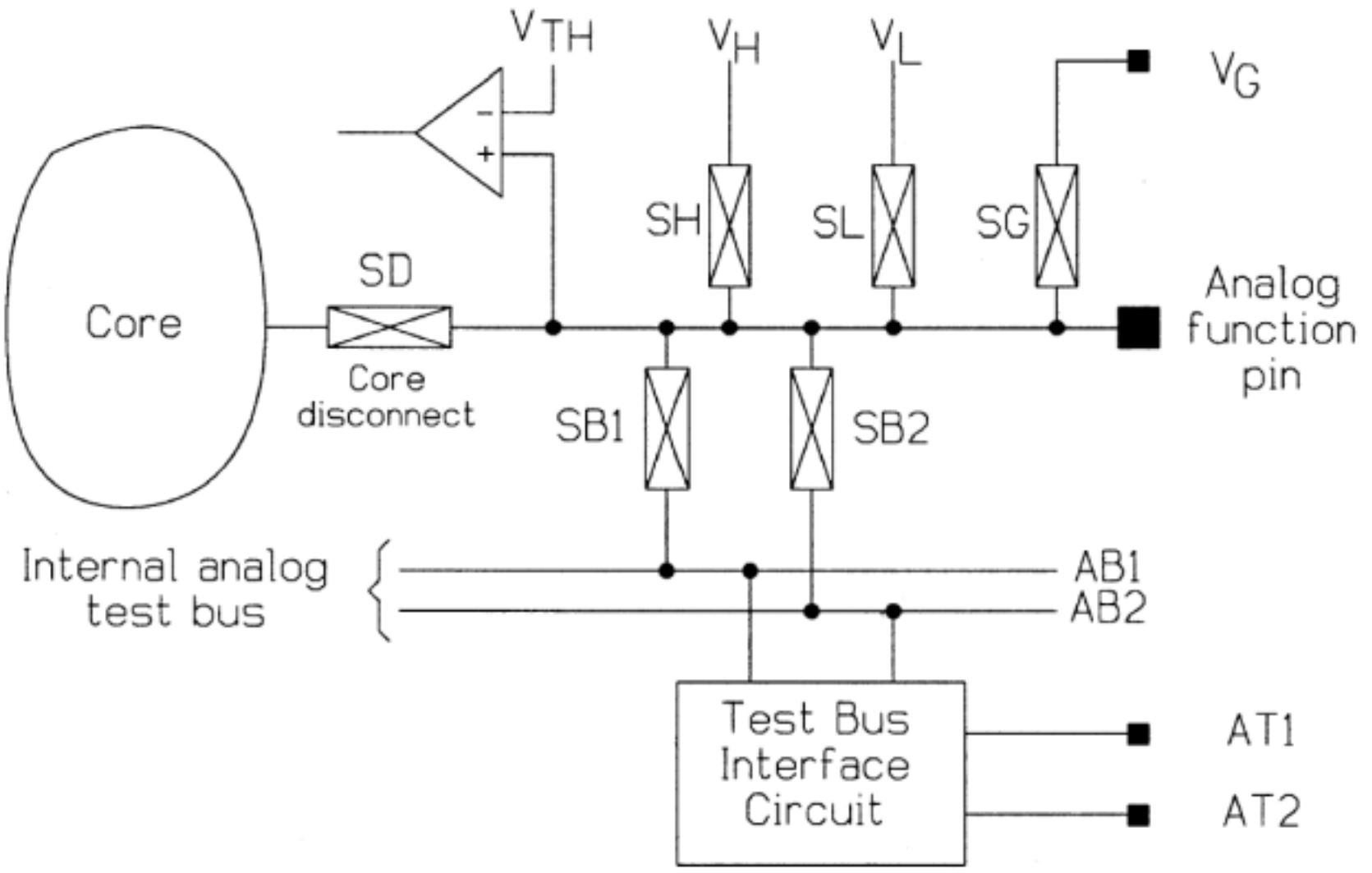
1149.4 Board-Level View



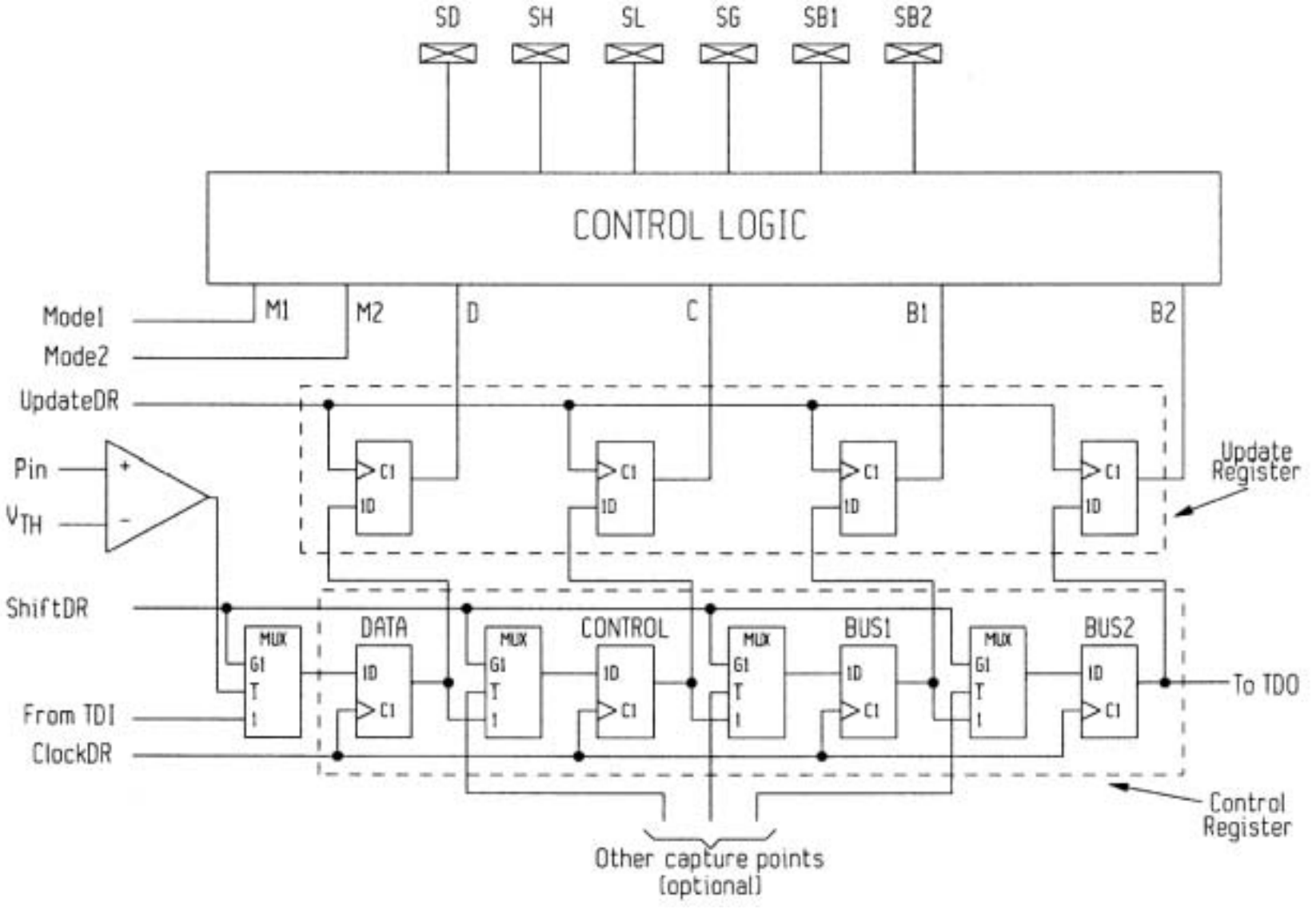
Test Register Architecture



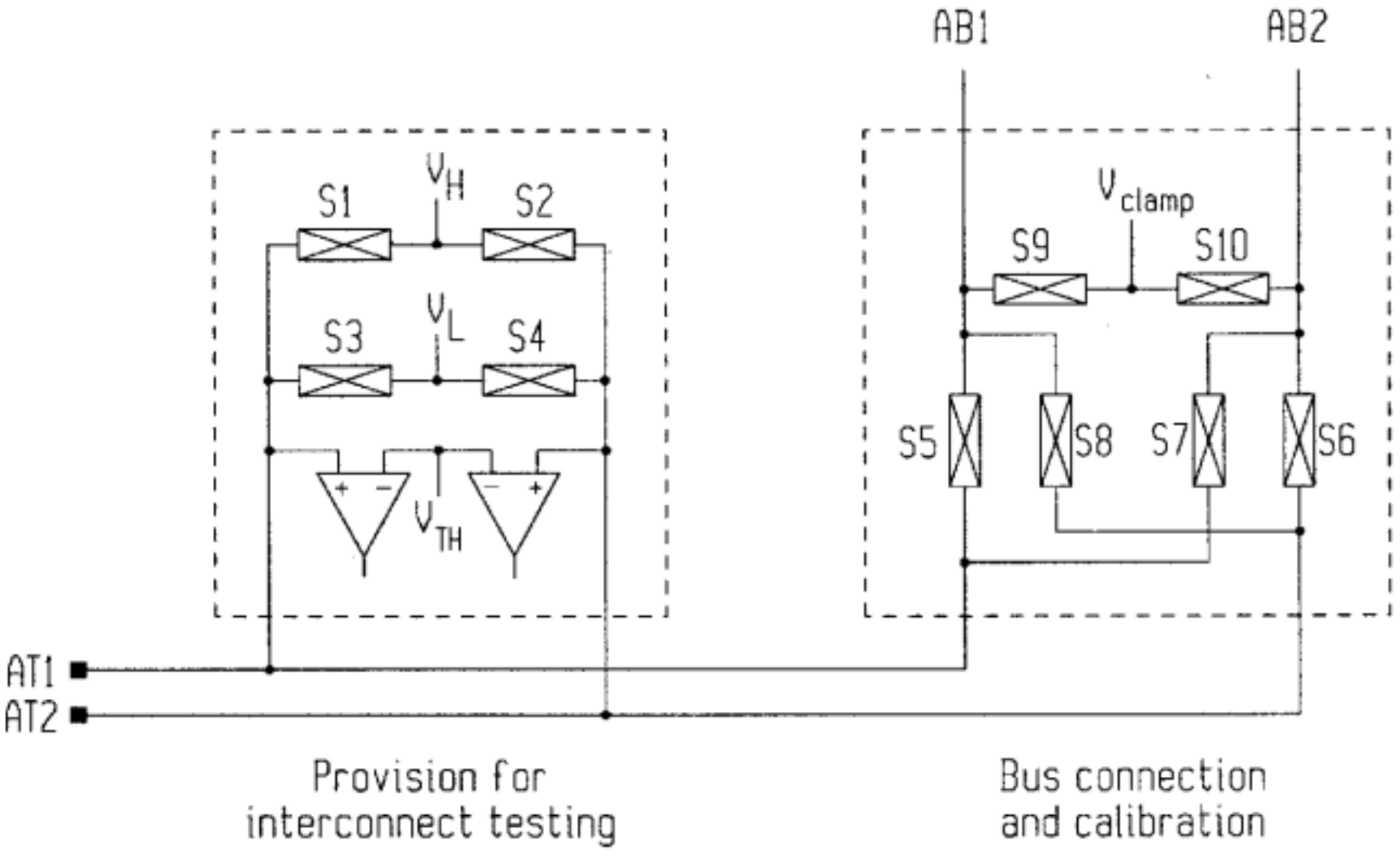
ABM Switching Architecture



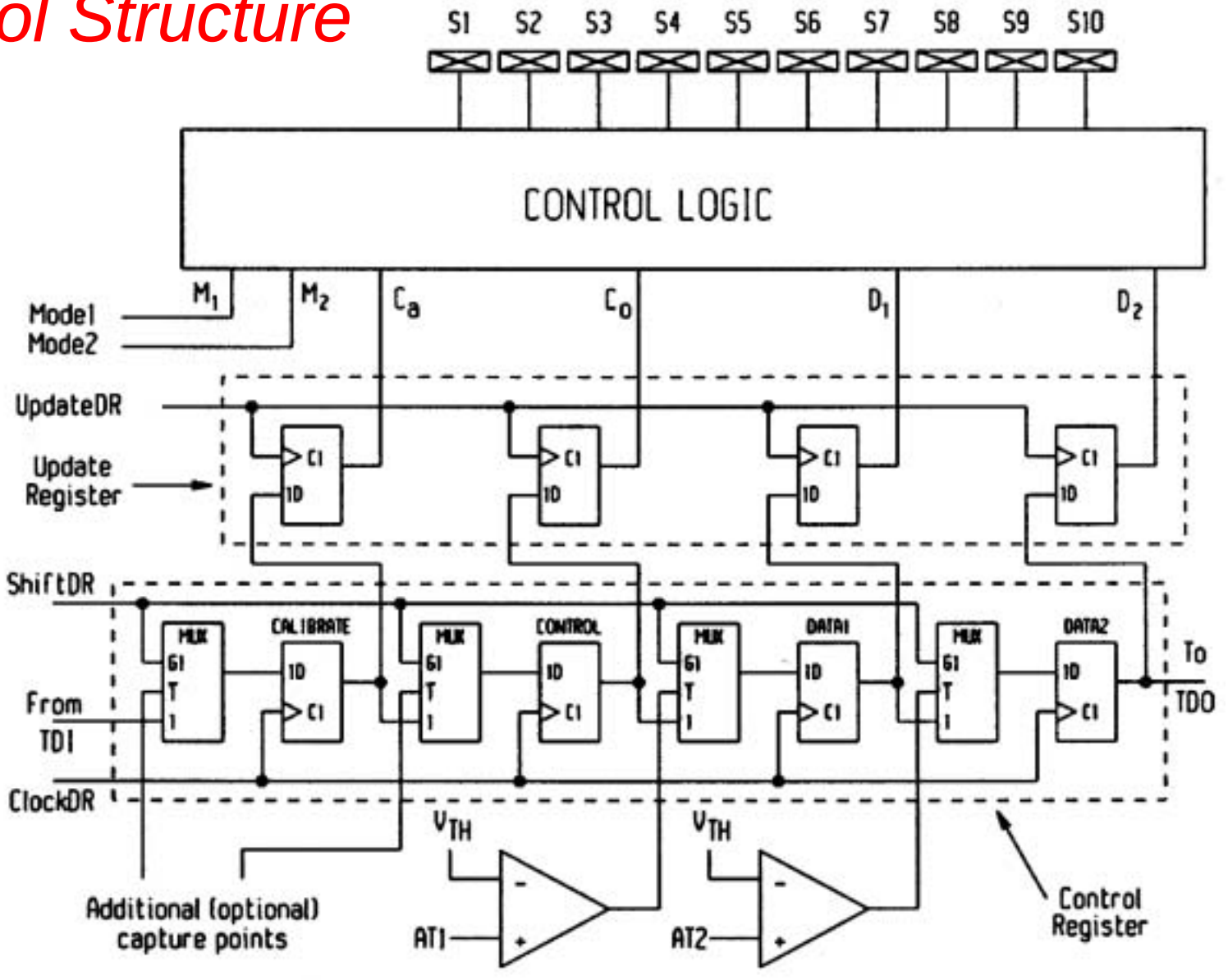
Possible Control Structure for ABM



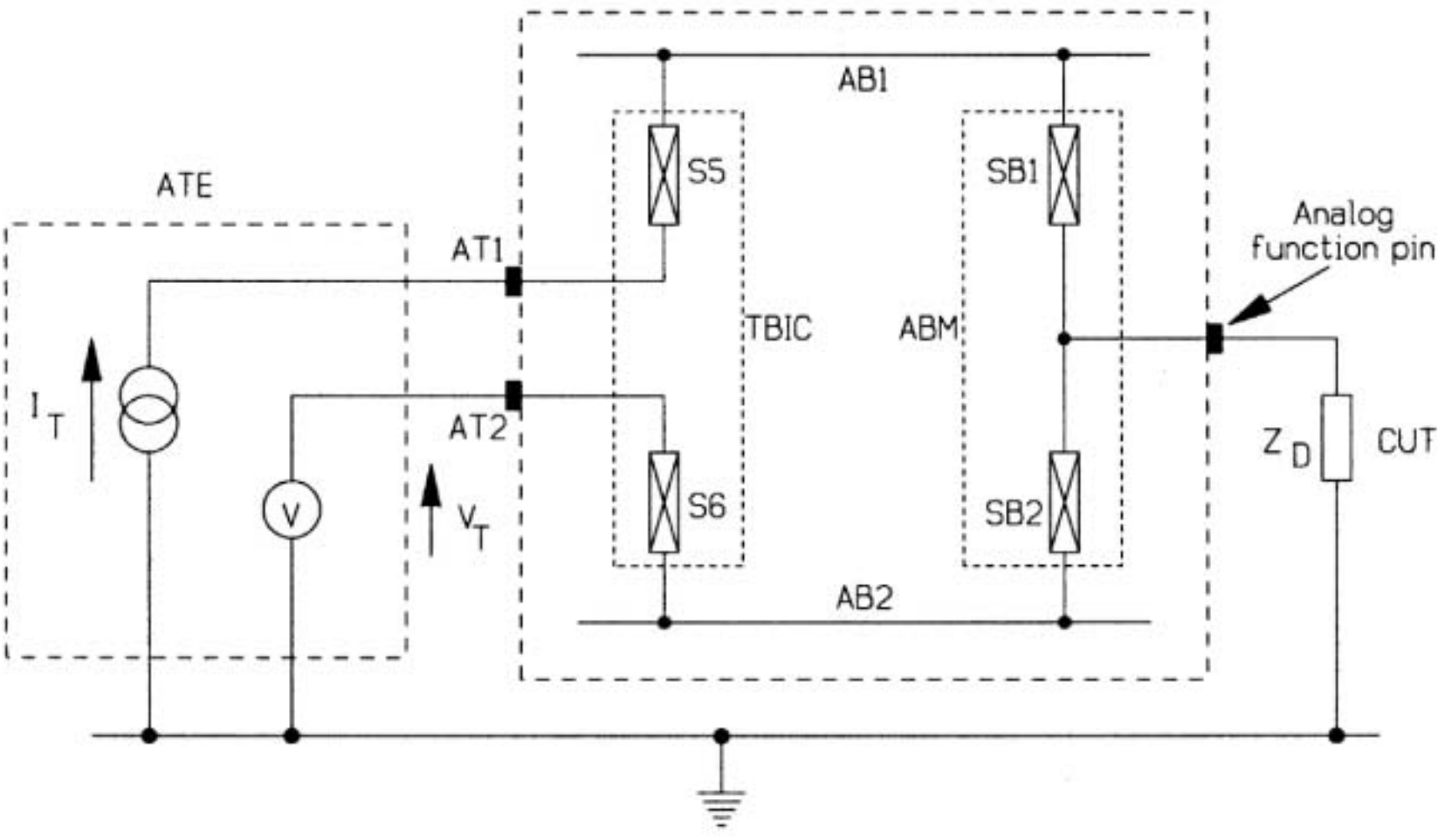
TBIC Switching Architecture



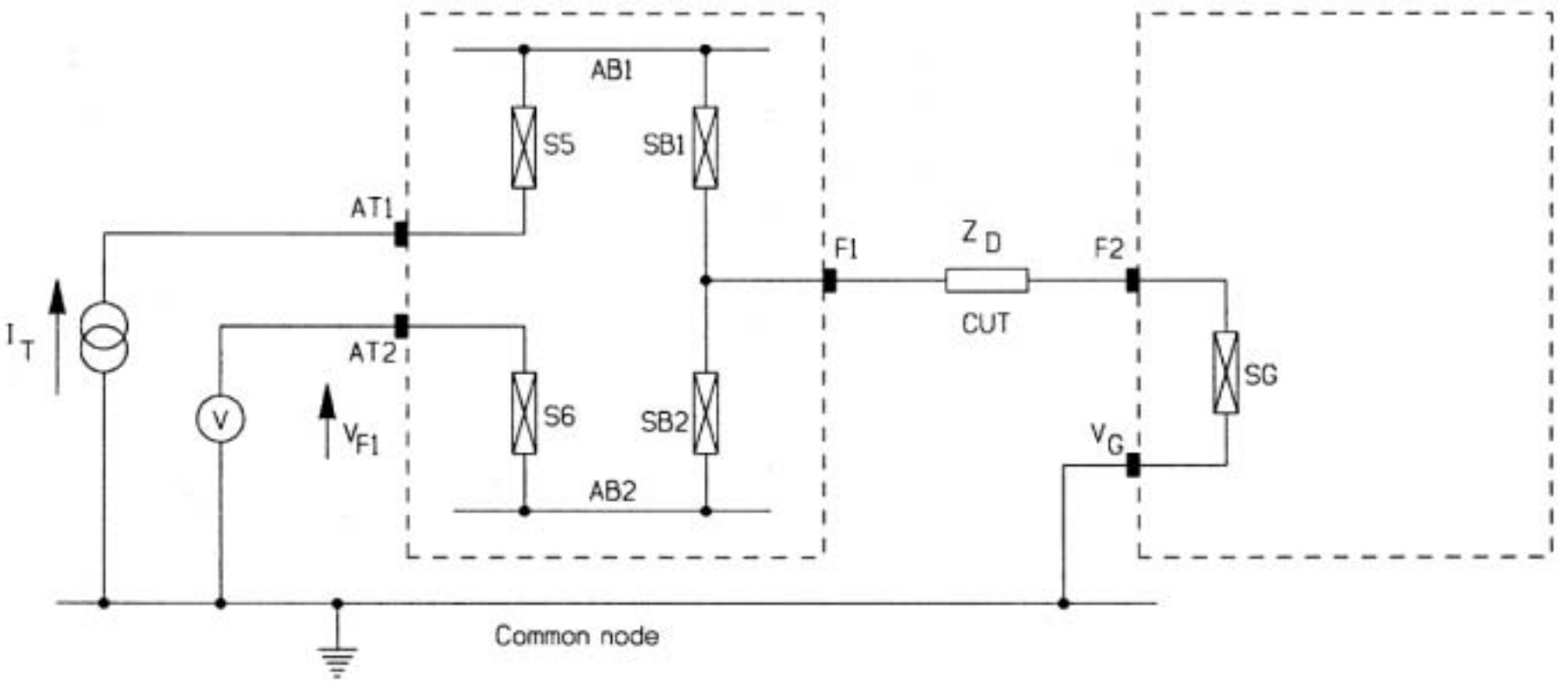
TBIC – Sample Implementation of the Control Structure



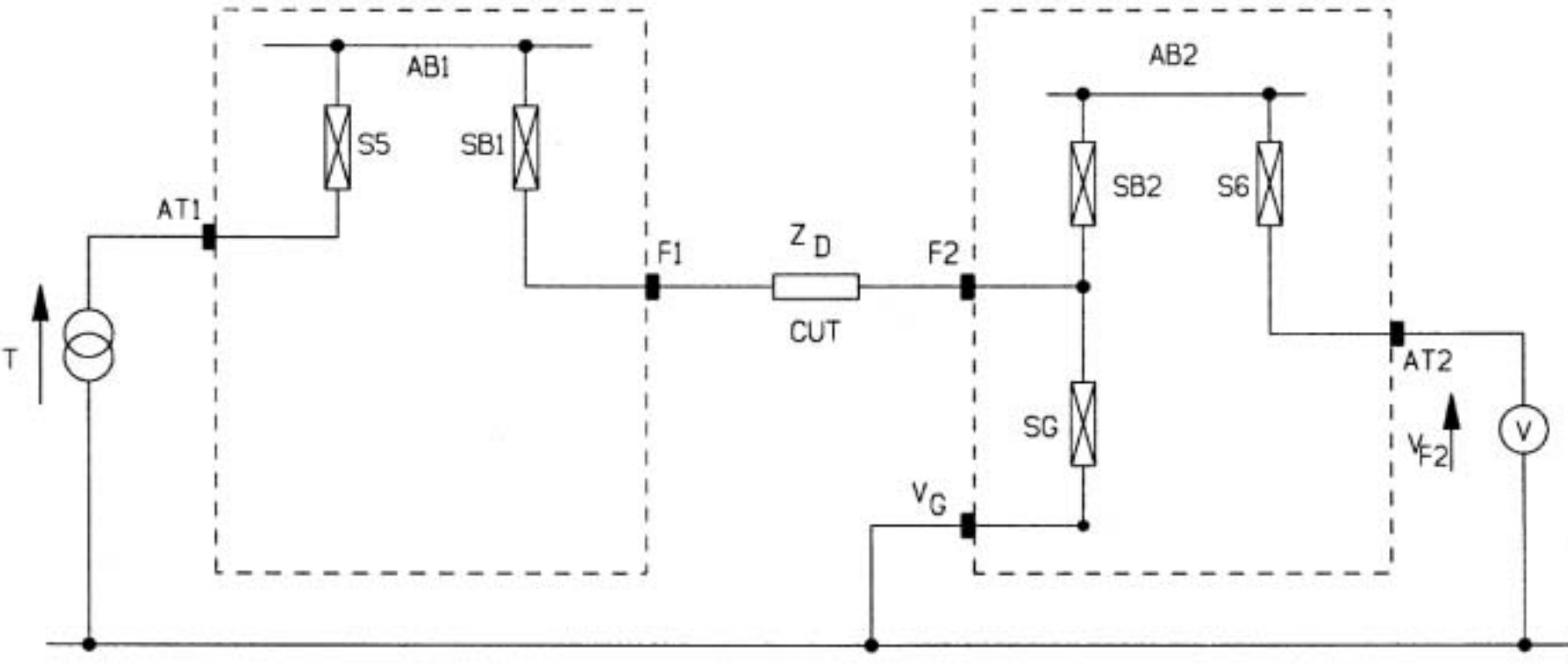
Virtual Probing



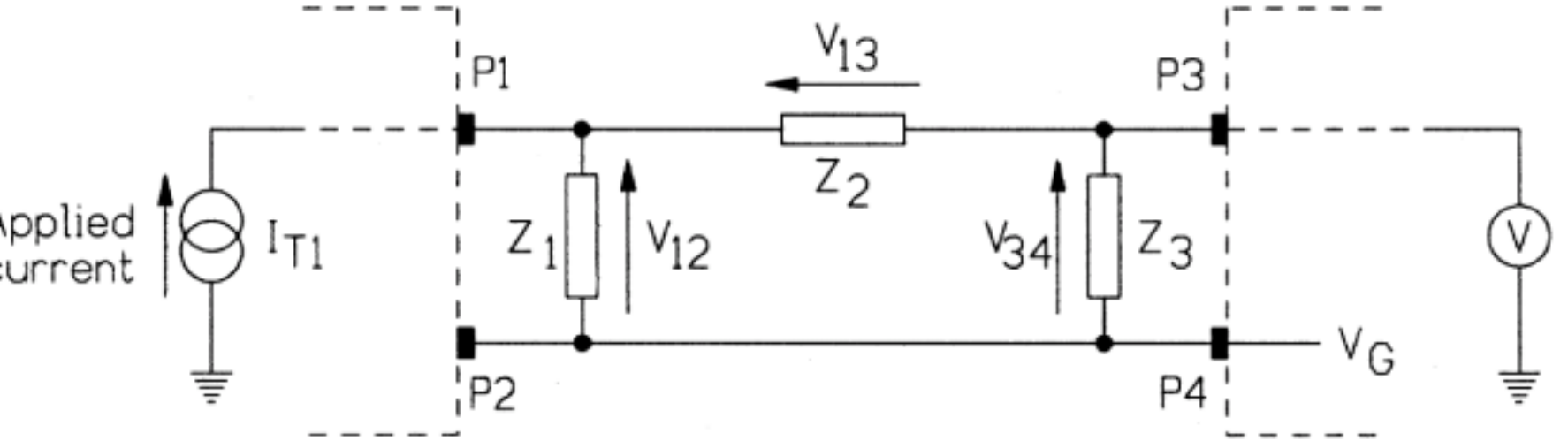
Extended Interconnect Measurement – Measurement One



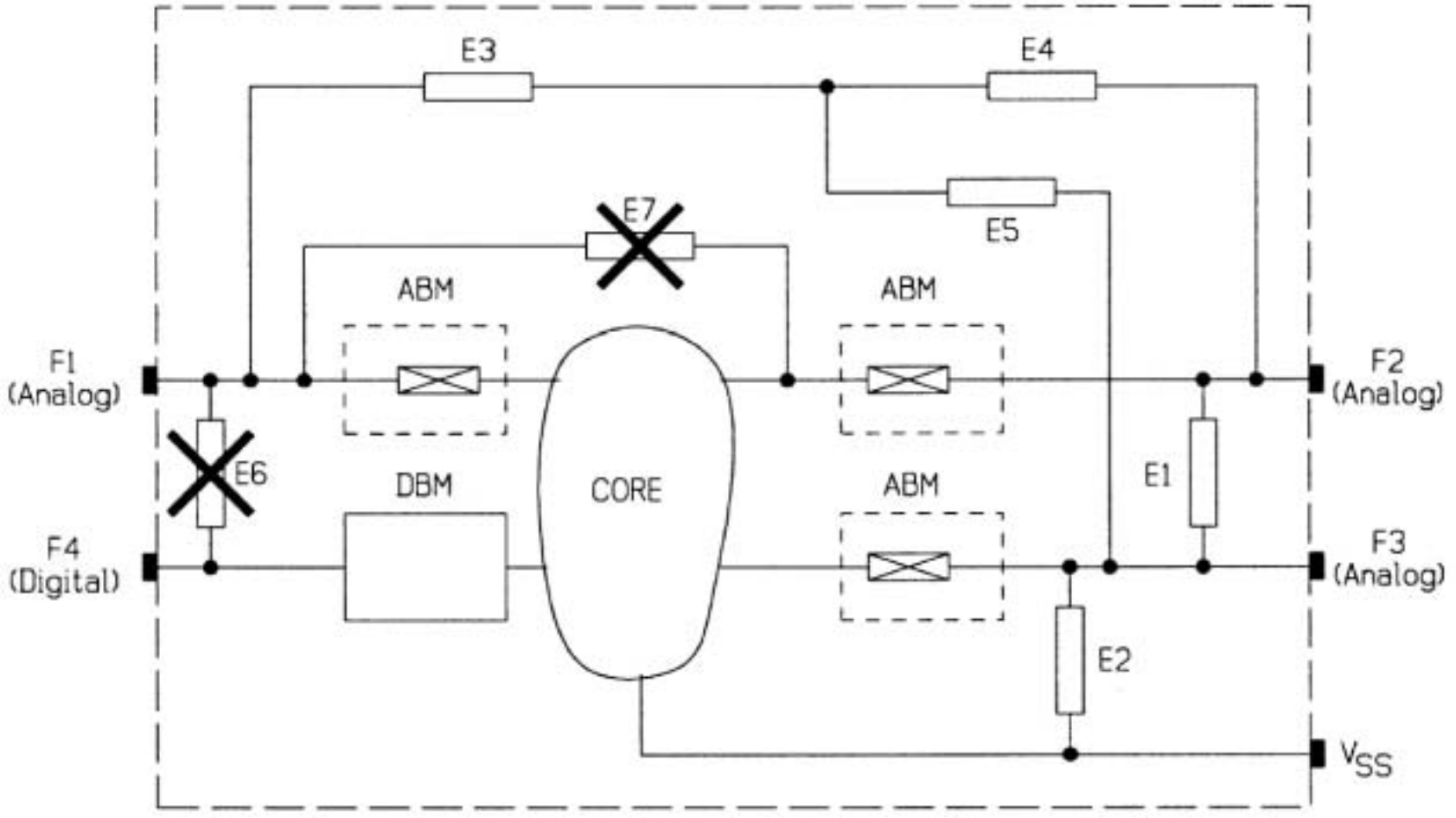
Extended Interconnect Measurement – Measurement Two



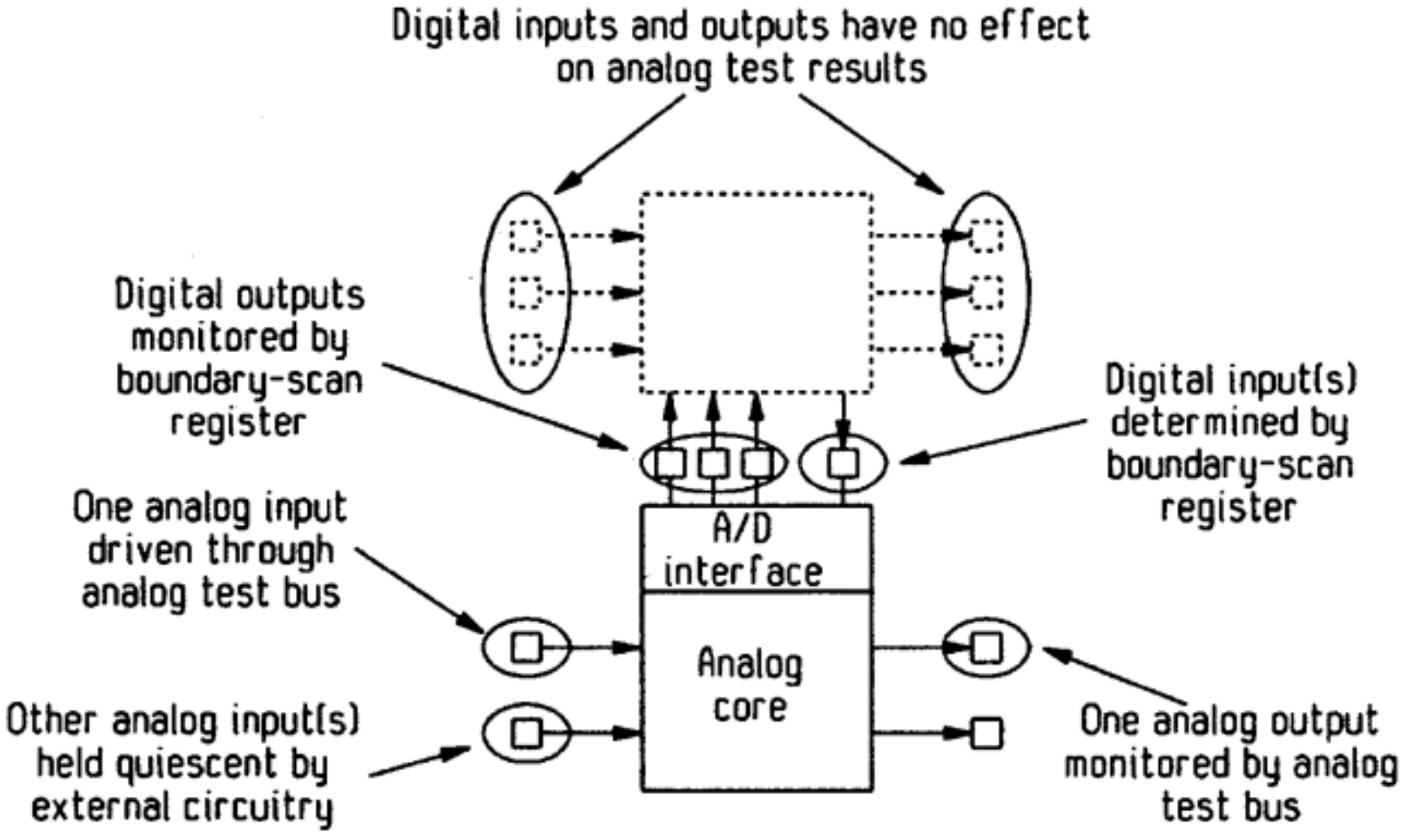
Network Measurement



Connectivity of Residual Elements

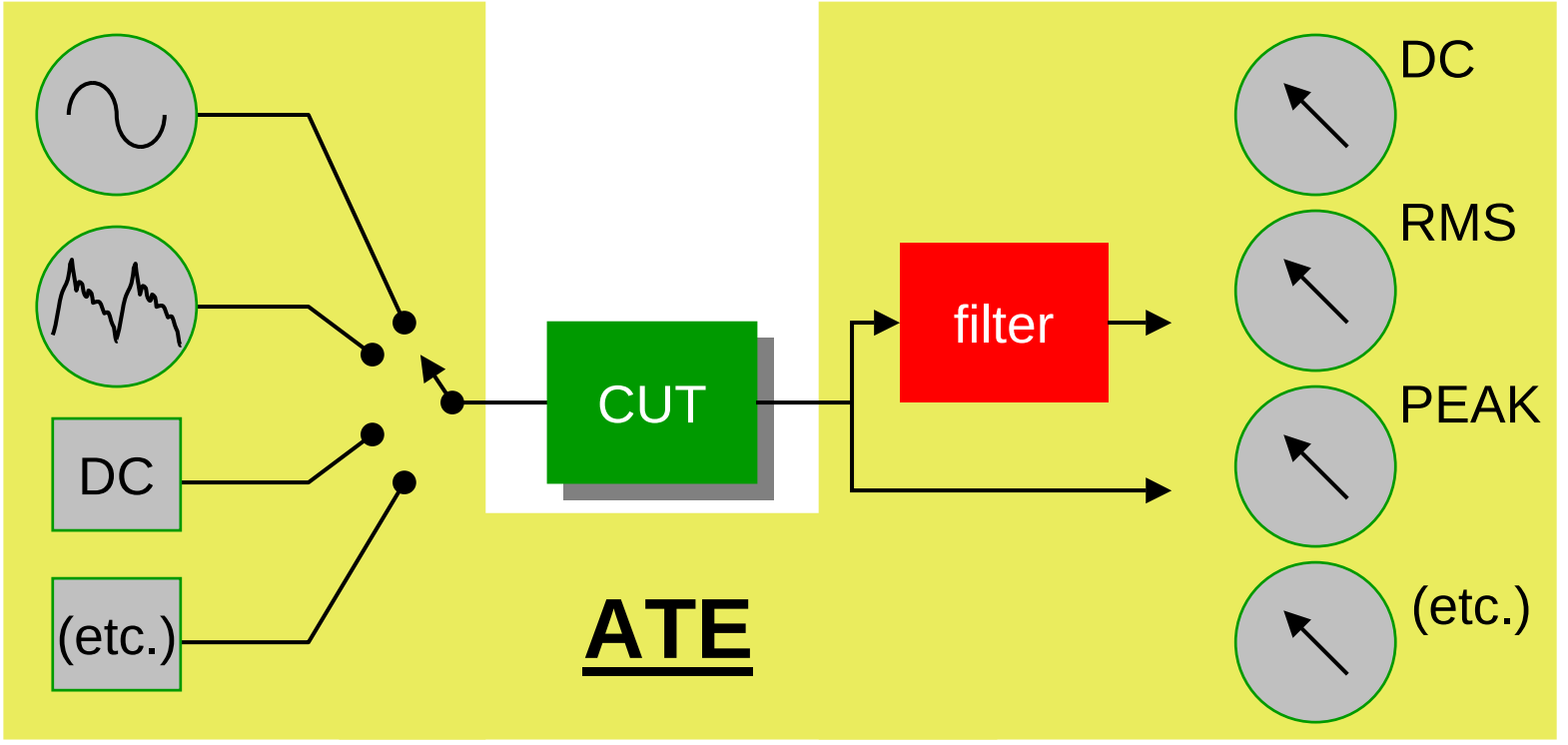


Testing the Analog Core



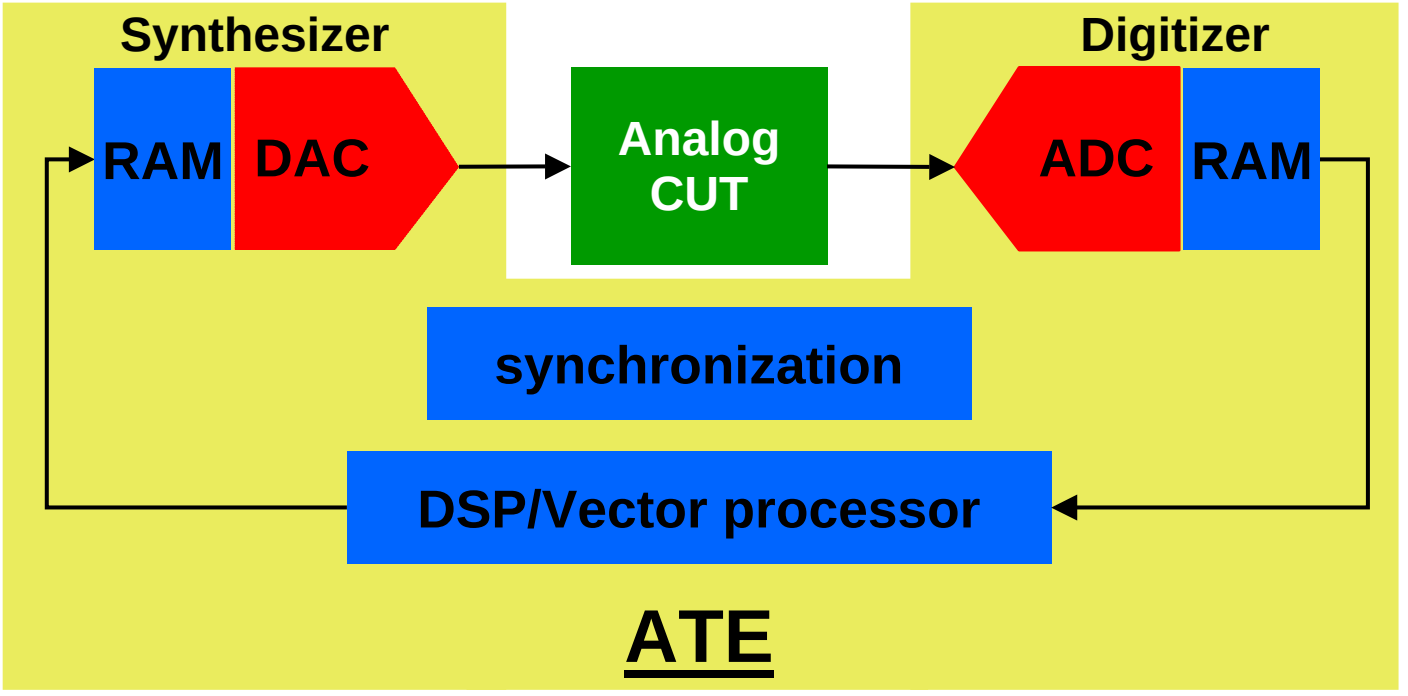
DSP-Based Mixed-Signal Testing

Analog Test Setup



- Low test throughput.
- Less flexibility.

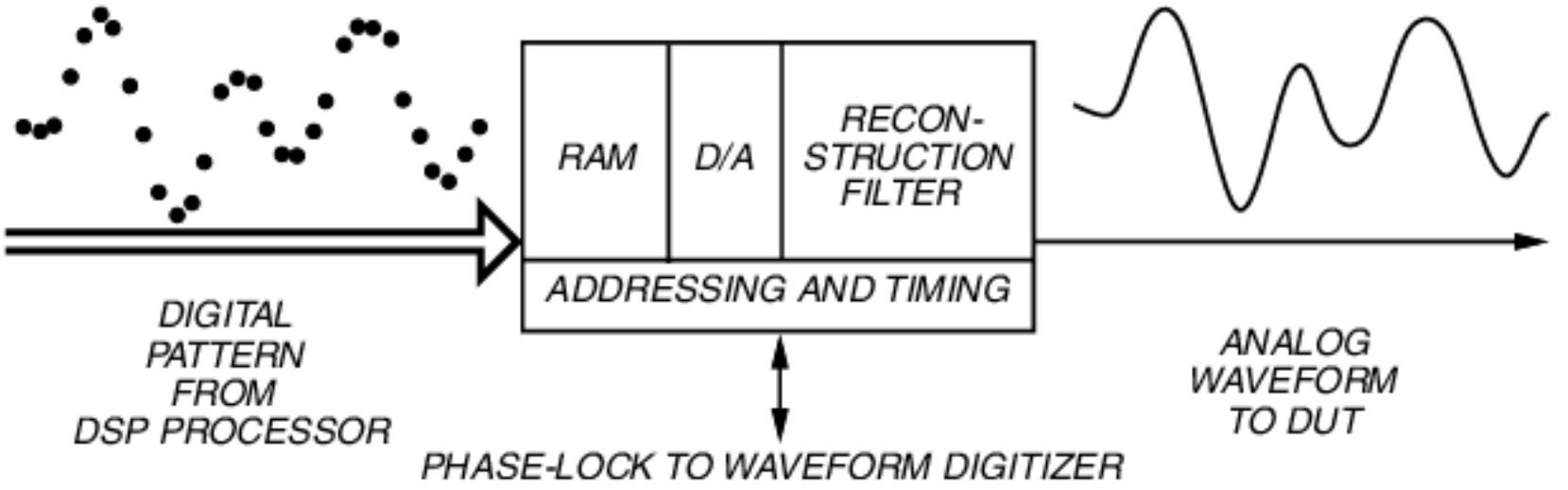
DSP-Based Analog Testing



- Flexible
  - single setup for multiple types of tests
- High throughput.
- Performance limited by ADC/DAC.

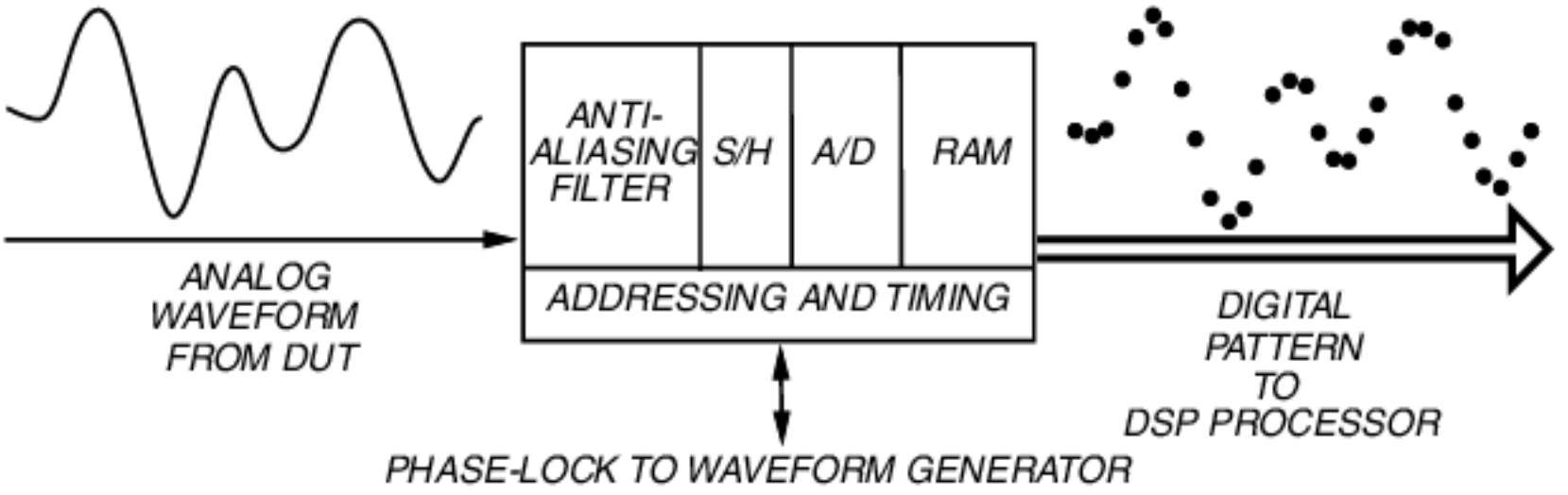
Test Waveform Synthesis

- Test signal
  - digitized sinusoid
  - digitized multi-tone
  - pseudo random



Output Response Digitization

- Response analysis:
  - FFT
  - IEEE 1057 sinewave fitting
  - cross-correlation / auto-correlation



DSP-based vs. analog ATE

- Increased test throughput
- Reduced switching & settling time
- Device response is memorized and analyzed for different parameters
- Software DSP doesn’t have to be real-time
- Performance limited by ADC/DAC

DSP-Based Mixed-Signal SoC Self-Testing

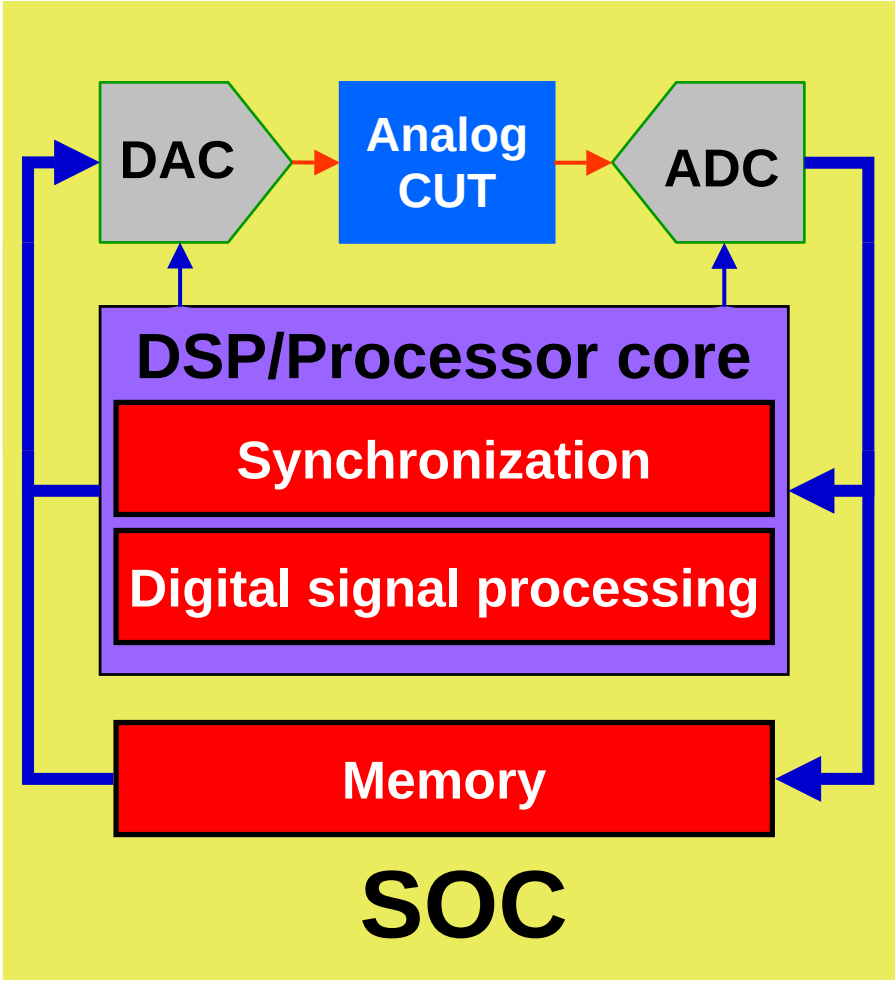
New Opportunities

- Utilize on-chip DSP capabilities to facilitate mixed-signal testing.
  - Test the digital parts first.

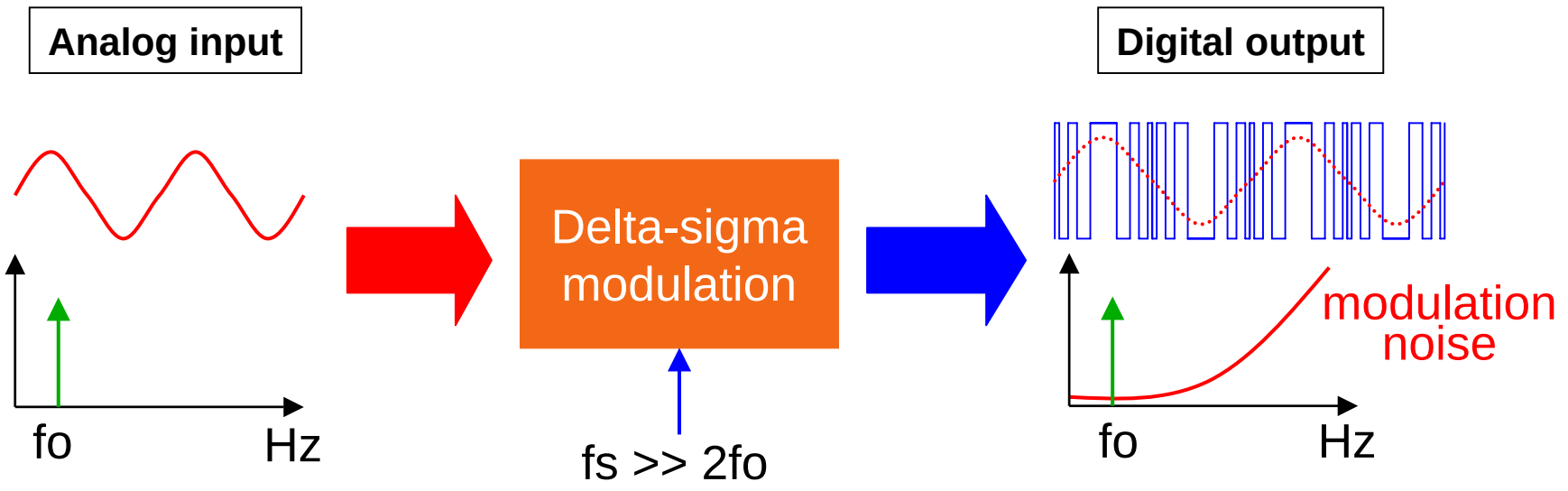
- On-chip ATE!!

DSP-Based Self-Testing of Analog Components

- DSP-based BIST – on-chip tester
  - Relieve the need of expensive ATE
  - Reduce external noise
- Practical issues
  - Test quality limited by DAC/ADC
  - DAC/ADC are not always available, and must be tested first



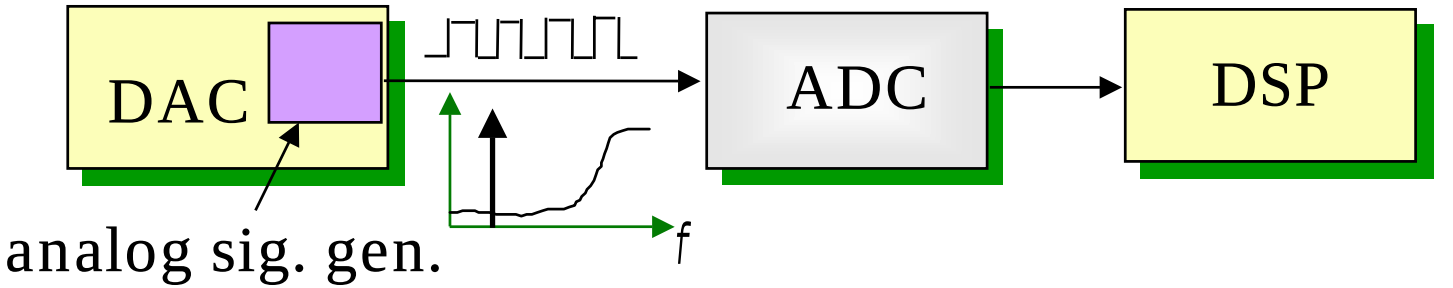
The Delta-Sigma Modulation



- High sampling rate (fs >> 2fo), low output amplitude resolution
  - Average output tracks input value
- Allows the use of relatively “imperfect” components
  - Suitable for VLSI implementation

MADBIST - Mixed Analog-Digital BIST

Testing ADC first!!



- Build a precision analog signal generator into the DAC:
  - high frequency, pulse density modulated single bit-stream using ΣΔ modulation technique
  - producing high-quality analog sinusoidal/multitone signal
- Could perform SNR, FR and IMD tests for ADC

Ref: Toner & Roberts, ITC93, VTS94

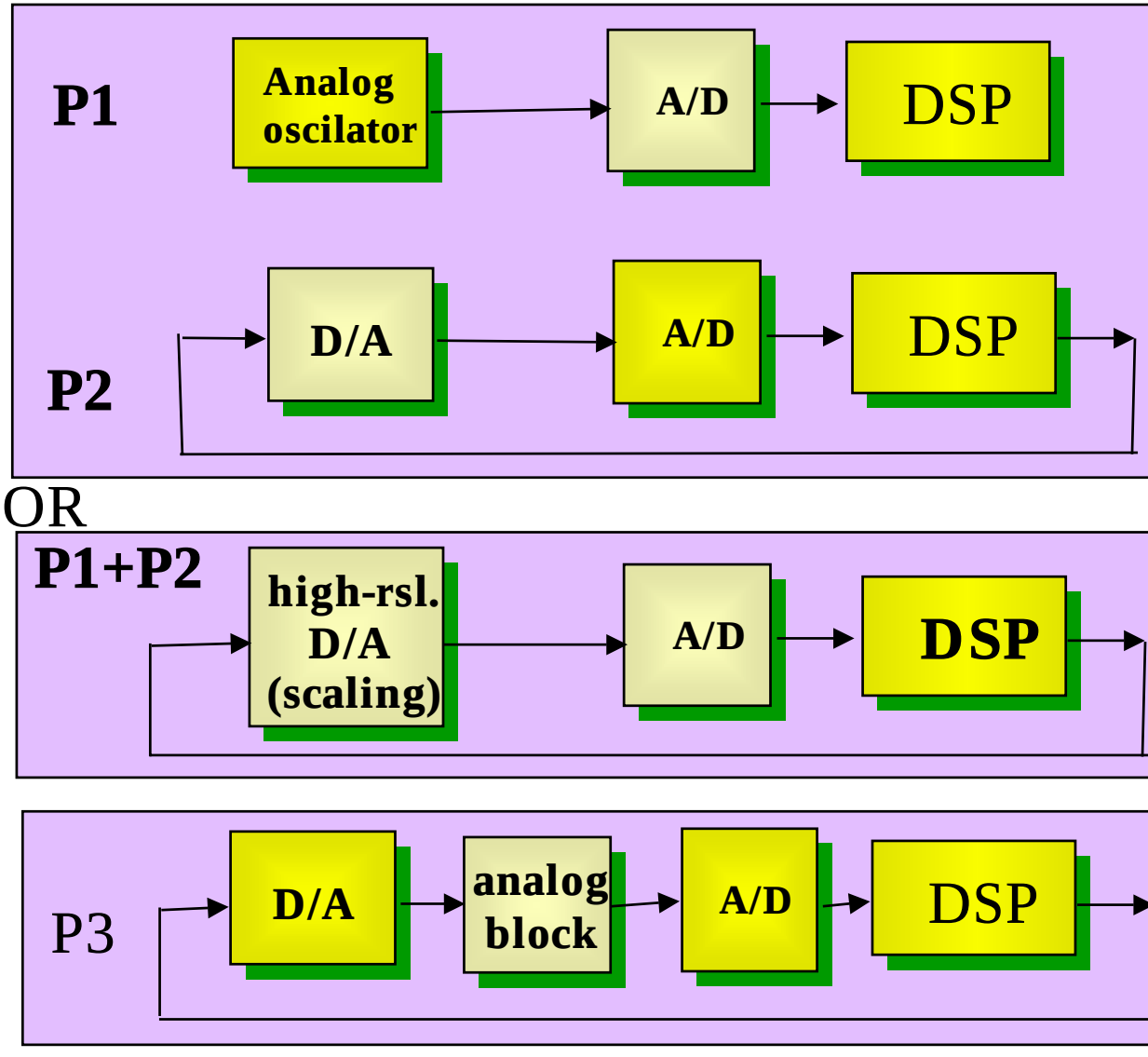
Multiple Test Phases.....

P0: Testing DSP

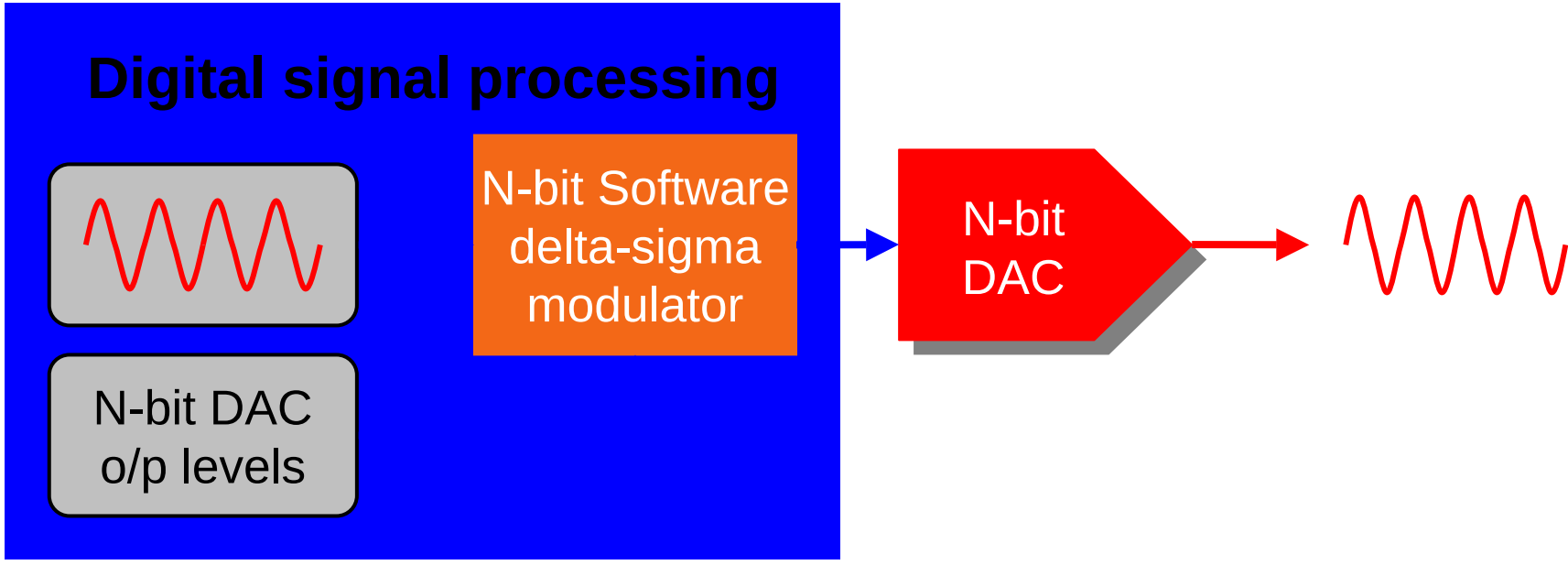
P1: Testing ADC

P2: Testing DAC

P3: Testing analog blocks

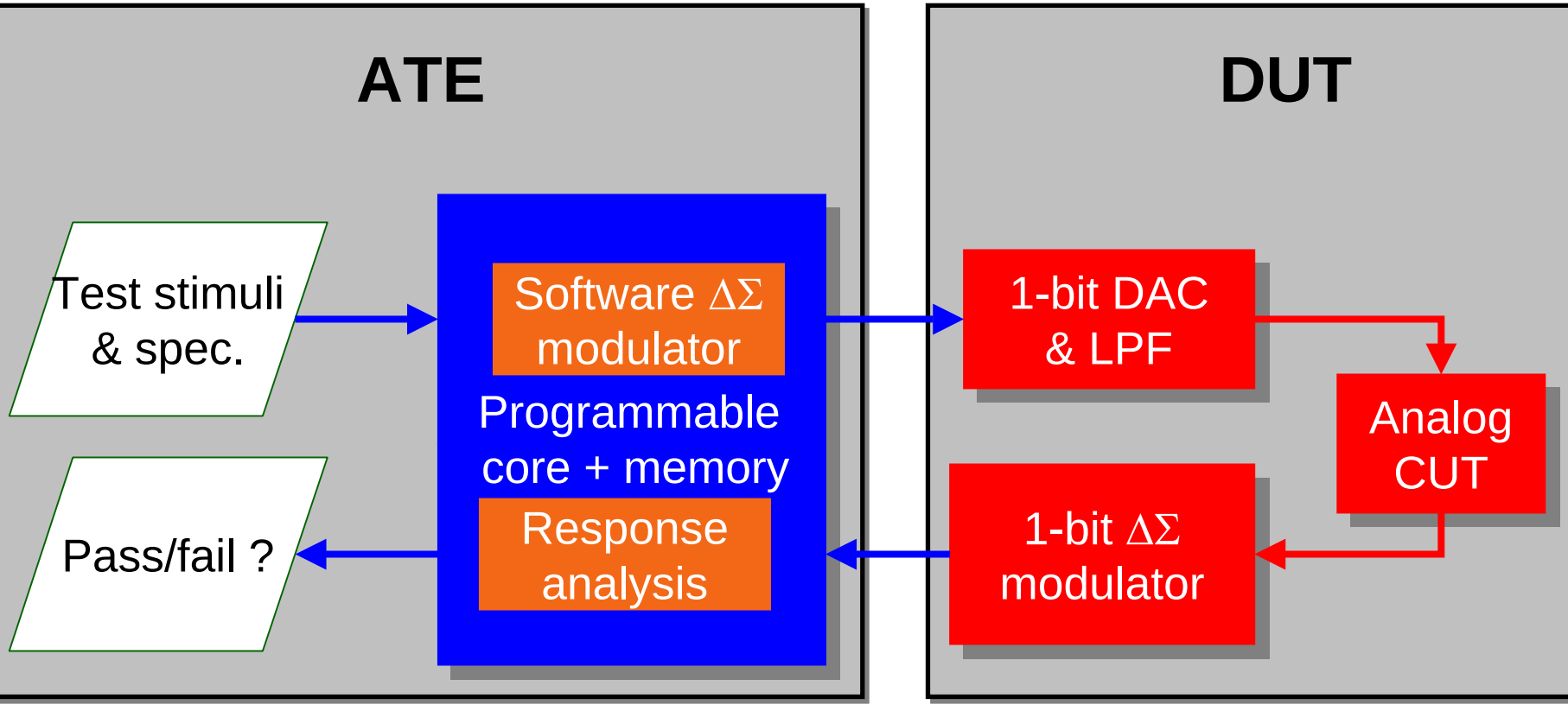


Delta-sigma Modulation Based Signal Generation [Roberts]

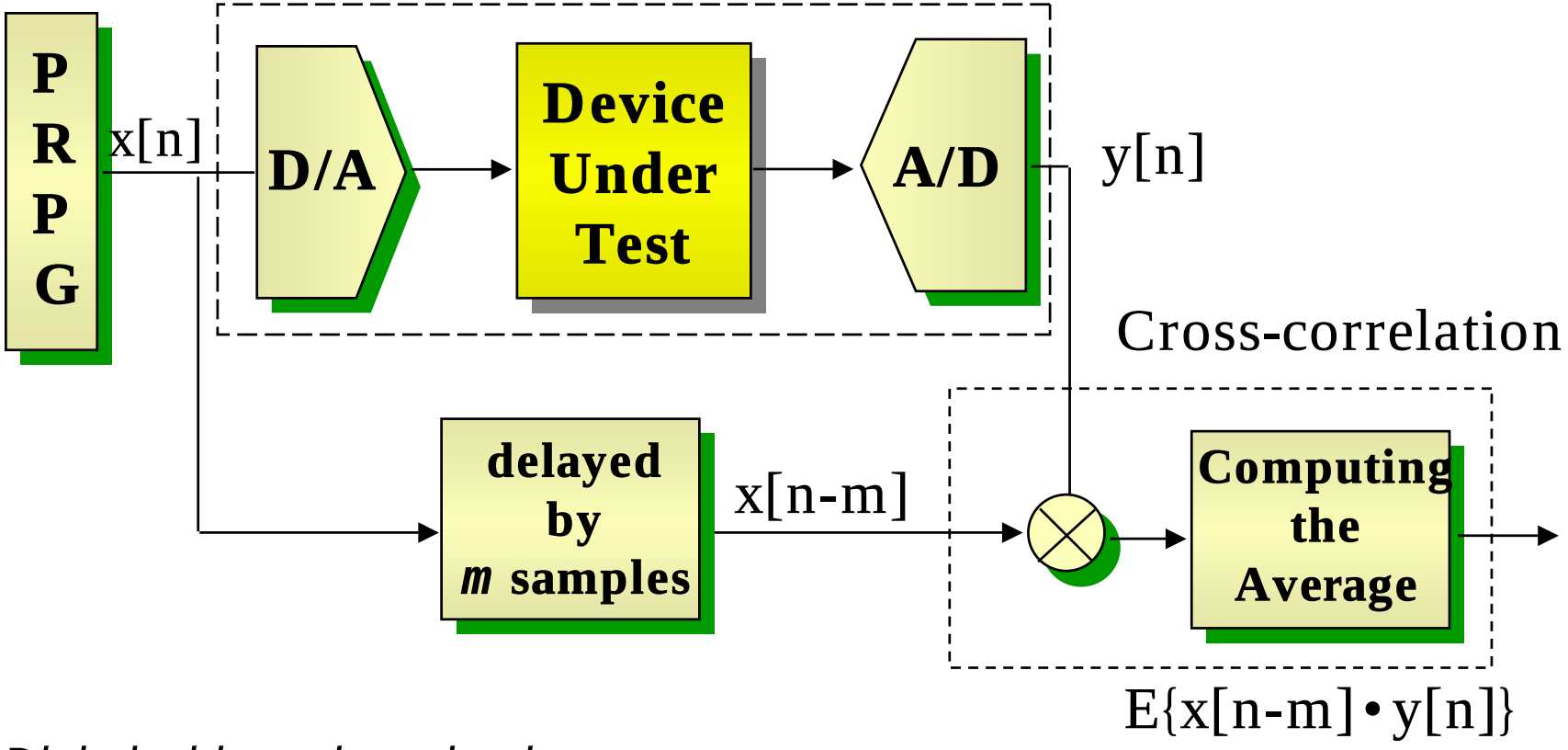


- 1+ bit in DAC → 6dB SNR gain
- How to measure the DAC output levels using on-chip resources?

Delta-Sigma Modulation Based BIST Architecture



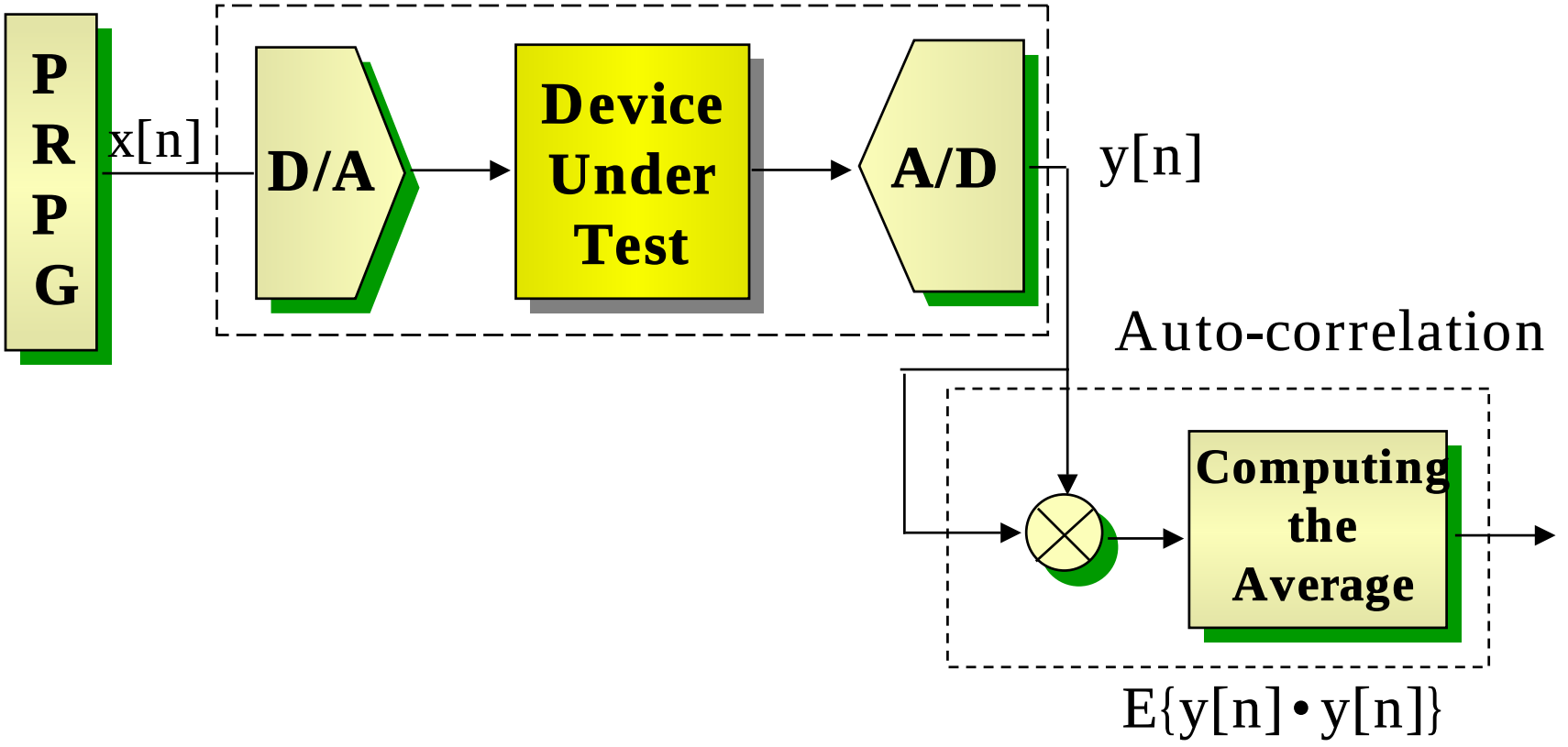
Pesudo-Random Testing



- *Digital white noise stimulus*
- *Testing multiple specs. in one test session*
- *Effective dynamic testing*

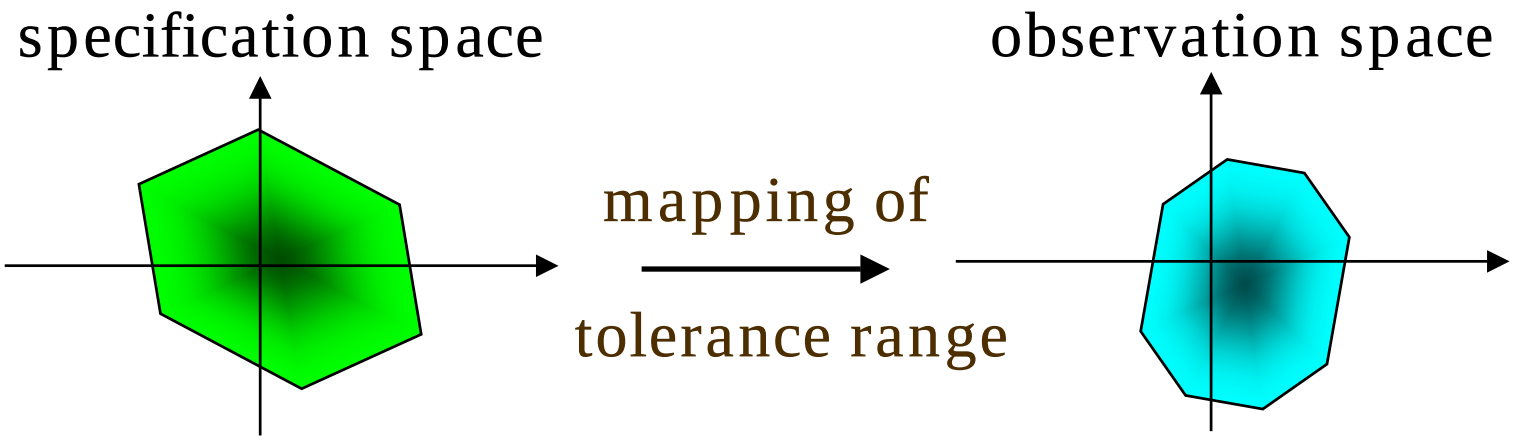
Ref: Pan & Cheng, ICCAD95

Pseudo-Random Testing



Ref: Pan & Cheng, ICCAD95

Automatic Mapping of Tolerance Range



- Tools for automatic mapping of tolerance range from the given specs. to the observation space are needed
- Perfect mapping may not be possible
  - Objective: minimize misclassification

Conclusion

- Although expected to lag leading-edge device performance and complexity, DfT techniques are essential to reduce dependence on expensive ATE.

- Need more research into the area of structure testing.
  - No proven alternative to performance-based analog testing exists.