Reliability of Bond Over Active Pad Structures for 0.13-μm CMOS Technology

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Abstract

Advances in CMOS (Complementary Metal Oxide Semiconductor) device technology have helped reduce typical die core sizes by shrinking the minimum transistor feature size. In the case of wirebonded devices with high IO counts, the final die size is increasingly determined by the size and layout of the IO cells and corresponding wirebond pads. Typical wirebond pad designs consist of a top-level metal that does not include any circuitry beneath the bonding region. Further, placement rules typically require the placement of ESD circuitry, buffers, and busses inside of the bond pad ring in order to avoid possible damage and reliability failures caused by wirebonding. On die with high pad counts, this exclusion area can represent a significant percentage of the die area that is not used for circuitry.

This papers describes a layout technology called *Bond Over Active* (BOA), that was developed to utilize this "excluded" region beneath wirebond pads in order to minimze die area. Two different BOA layouts are evaluated using a standard test structure. Wirebond assembly reliability and package stress reliability are determined. The transfer of forces from the top metal pad to the active silicon during wirebonding are predicted using mechanical simulations. The results of the simulations are used to explain the similar levels of reliability observed for the two BOA layouts.

Introduction

Die size reduction is a top priority for cost competitiveness. Advances in CMOS (Complementary Metal Oxide Semiconductor) device technology have reduced typical device geometries to 0.13-μm. Die core sizes have decreased concurrently. In the case of wirebonded devices with high IO counts, the final die size has become determined mainly by the size and layout of the IO cell and its corresponding wirebond pad. Typical wirebond pad designs consist of a top-level metal that does not include any circuitry beneath the bonding region. Further, placement rules typically require the placement of ESD circuitry, buffers, and busses along the inside of the pad ring in order to avoid possible damage to these active structures during wirebonding. On die with high pad counts, this exclusion area can represent a significant percentage of the die area that is not used for functional circuitry.

In order to utilize this excluded area, several pad structures have been proposed in previous studies [1-3]. These evaluations focused on the incorporation of stress absorbing or dissipating layers below the bond pad to mitigate the forces applied to the pad during wirebonding. The placement of vias in the region under the pad for mechanical reinforcement was studied for Al/low-k interconnect structures [4]. This work examined only the mechanical response of the pad structures. The effect of wirebonding over ESD structures was assessed for 3-metal layer copper/SiO_2 interconnect technology [5]. In addition to physical evaluations of pad designs in silicon, this work also included simulations of the effect of wirebonding on 3- and 5-metal pad structures that provided predictions of the distribution of the stresses resulting from wirebonding.

In this work, a layout technology, termed *Bond Over Active* (BOA), was developed to allow the placement of wirebond pads over active silicon without the addition of reinforcing layers. These BOA layout methods allow the inclusion of multi-level metal wiring, vias, and contacts in the sub-pad region. Placement these active elements under the bond pad allows the movement of the wirebond pad over the power and ground busses, diodes, MOSFETs, and ESD structures at the periphery of the die core. BOA layout offers higher levels of integration that can result in a significant reduction in the overall size of the die.

Experimental Approach

The evaluation of the pad structures with bond over active layouts was conducted in three stages:

(1) assembly reliability, where the effect of wirebonding forces on the function of the BOA structures was assessed;
(2) package reliability, where the failure rates in standard package qualification stresses were determined; and,
(3) mechanical simulation to examine the relative effects of elements within the pad structure on the stresses developed during wirebonding.

Test Structures

The elemental test structure for this work consisted of a group of six bonding pads, termed a *six-pack*. The six pads of the structure included a power, ground, two input, and two output pads (Figure 1). The two input pads were wired to the n- and p-channel inputs of a CMOS inverter as described in Figure 2. All of the pads included at least a protection diode and a connection to the device ESD structures.

These six-pack test structures were incorporated into a peripheral pad ring on a carrier die. Each six-pack was electrically isolated from the others on the die, allowing them to be independently tested. Each structure was repeated on all

four sides of the die so that the direction of wirebond forces could be factored.

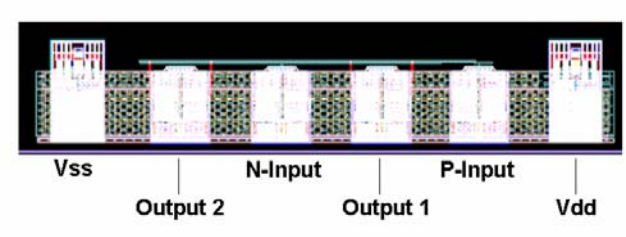

Figure 1. Bond Over Active Test Six-pack Layout

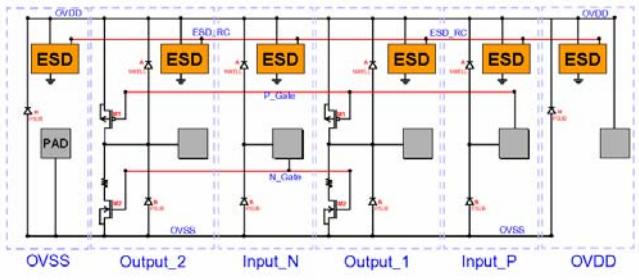

Figure 2. BOA Test Circuitry

In this study, two different six-pack test structures were evaluated with different densities of circuitry in the region below the wirebond pad. Representative drawings of the major features of these two BOA layouts, called BOA Type A and BOA Type B, are shown in Figures 3 and 4.

The A-type BOA layout features active silicon, such as diodes and transistors, located under the passivation opening. However, within the region below the passivation opening, the metal wiring and vias were placed only at the lowest levels in the stack that are needed for routing. Vias and contacts in adjacent layers were offset from each other in order to minimize the direct transfer of forces from the last metal pad during wirebonding.

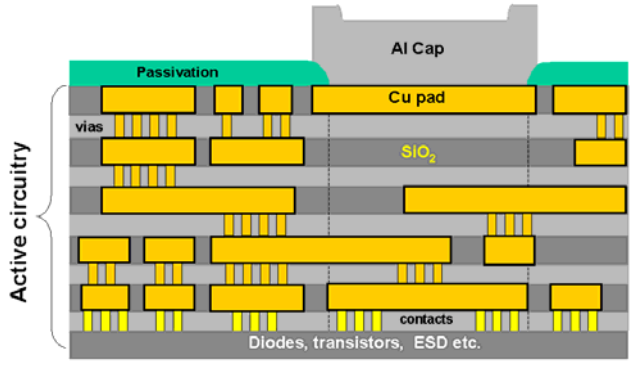

Figure 3. Bond Over Active Type A

The BOA-B layout features the maximum metal density possible within the passivation opening. All four metal levels below the last metal pad are populated and connected by stacked vias. These via stacks are in turn stacked over the contacts over the active silicon below. Mechanically, this layout presents the most direct path to transmit the wirebonding forces to the active silicon and presents the most likely structure to cause functional failures. Pad Type B was expected to present the worst-case placement of active circuitry, as the wirebonding forces were expected to transfer directly from the bonding pad to the active silicon.

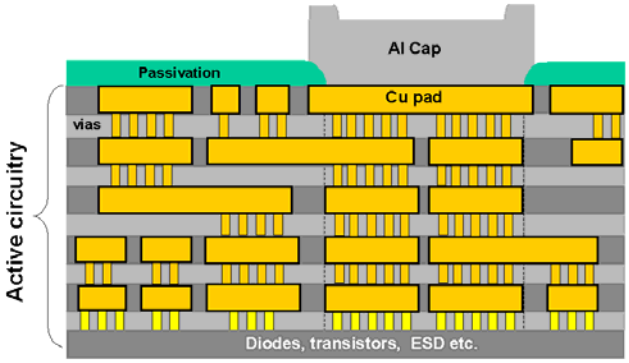

Figure 4. Bond Over Active Type B

The test vehicle die was fabricated using 0.13µm CMOS process technology and featuring five layers of copper metal/ SiO_2 interconnect. The last metal pads were capped with aluminum for wirebonding. The bond pads were designed to 65µm fine-pitch wirebond pad specifications, but were placed at 110µm final pitch to aid in testing and failure analysis. The final die size was 6.45mm x 6.45mm.

The test program was developed to determine continuity to each bond pad by sensing the drop across the pad protection diodes on each pin. Shorts between pads and/or wires were detected by applying voltage and ground to alternating pins and sensing current drawn. Leakage through the p- and n- channels was measured in the off and indeterminate states to detect any damage to the gates below the wirebond area. Leakage paths between metal lines, between adjacent busses, and between the pads in the six-pack were also tested.

Assembly Reliability of BOA Pad Structures

Standard process flows were used for probe and assembly to reduce the variables in the evaluation and focus on the pad structures. The wafers were probed using a commercial automated wafer prober and cantilevered needle probe card. Overdrive for the probe card was set at 50µm and the probe operation was completed in one double-touch pass to minimize the size of the probe marks. The probed wafers were processed using a standard production flow for backgrind, ink, and saw. The known good die were sawn from the wafers, bonded to organic substrates, and then plasma cleaned prior to wirebonding. Wirebonding was completed commercial wirebonder with 1.0 mil diameter gold wire, targeting a 48-50µm bonded ball diameter.

In order to assess the wirebond assembly window of the BOA structures, two sets of wirebonding conditions were used (Table 1). The standard fine-pitch wirebonding parameters for Al-capped-Cu bond pads were used for the baseline, or normal, assembly stress. The second set of wirebond parameters was derived by increasing the capillary impact and holding forces by 25% and increasing the ultrasonic power by 15%. The bonded ball sizes for the

standard and high wirebond conditions were between 48µm and 52µm. A total population of 679 die were assembled: 285 using the normal wirebond parameters and 320 using the high wirebonding force/power. This yielded totals of 1140 and 1280 BOA six-pack test structures for the standard and high wirebond conditions, respectively. Finally, the wirebonded die were molded in a 256 lead, 17x17x1.3mm 1mm pitch PBGA for testing and package stresses.

	Normal Wirebond	High Wirebond
Force	Center of window	Center + 25%
Power	Center of window	Center + 15%

	Functional Failures As-Assembled	
BOA-A	0/1140	1/1280
BOA-B	0/1140	1/1280

Table 1. Assembly Reliability for BOA Types A and B.

Functional testing results of the as-assembled packaged units are summarized in Table 1. The "high" wirebonding stress cell of the study yielded only one functional failure for each of the Type A and Type B six-pack structures. These two failures were physically located on one side of the same packaged test die. Both of these six-packs failed diode continuity, indicating an open condition between the tester and the protection diodes on the pads.

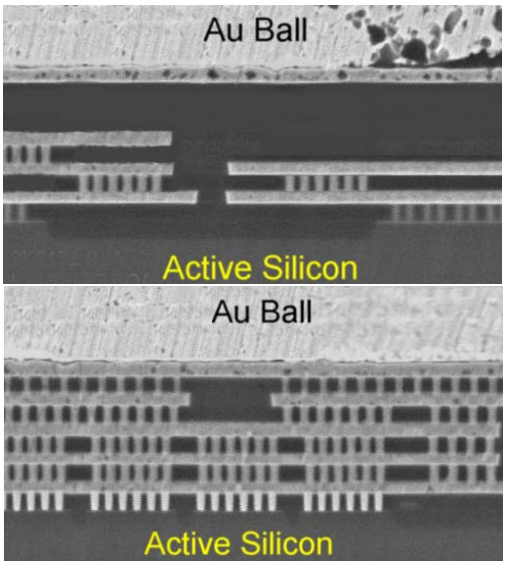

Figure 5. Cross-Sections Through Wirebonded Pads: BOA Type A (top) and BOA Type B (bottom).

Inspection of the packaged die by x-ray confirmed the presence and proper location of all six wirebonds on each of the failing six-pack structures. Due to the close proximity of the two failures, a gross die crack or delamination was the suspected failure mechanism. The die was sectioned through the entire pad row to examine for mechanical damage. Several section planes were inspected, including ones through the outer bonded ball edge, the ball center and the inner ball edge. Figure 5 is representative of the condition of the interconnect structures for each BOA pad type. No cracking or delamination was observed in any of the sections through the pad.

Based on the differences in the pad structures, particularly the stacked vias and contacts in BOA type B, greater differentiation was expected at wirebonding. The packaged die were subjected to temperature cycling and autoclave stresses in order to assess the reliability of the layouts in product. The application of package stresses, thermal cycling in particular, was expected to propagate non-catastrophic wirebonding damage that did not cause an immediate electrical failure.

Package Stress Reliability of BOA Pad Structures

In addition to wirebond mechanical response and post-assembly functional testing, the packaged BOA structures were subjected to typical product qualification package stresses. Package level reliability tests began with a 24 hr bake at 125°C, followed by Moisture Sensitivity Level 3 (MSL3) preconditioning. The MSL3 flow comprised: (1) 10 temperature cycles of -65°C to +150°C, (2) a 125°C bake for 24 hrs, (3) a moisture soak at 30°C/60%RH for 192 hrs, and (4) 3 reflow cycles at a maximum temperature of 240°C. After MSL3 preconditioning, one population of parts from each wirebonding condition was subjected to Temperature Cycling (condition C: -65°C/+150°C) with testing readpoints at 200, 500, and 1000 cycles. A second population for each wirebond condition was subjected to Autoclave (121°C, 100%RH, 15 psig) with testing readpoints at 96 and 144 hrs. A summary of the test structure populations and functional failures recorded at each package stress readpoint is given in Table 2. In addition to electrical testing, the packages were inspected visually and by CSAM in thruscan mode to check for package delamination. Package delamination was identified in several of the units in the 144 hr Autoclave populations. These units initially failed leakage testing, but passed retesting after a 24 hr bake at 125°C. Although the package material set was not optimized for this study and some delamination occurred, both of the pad types were mechanically robust enough that no functional failure was recorded.

	WB Force	Autoclave Stress Failures	
BOA Type		96 hrs	144 hrs
A	Std	0/568	0/568
B	"	0/568	0/568
A	High	0/640	0/640
B	"	0/640	0/640

Table 2. Autoclave Reliability for BOA Types A and B.

	WB	Temperature Cycle Stress Failures		
Pad:	Forces	200 cycles	500 cycles	1000 cycles
A	Std	0/572	0/572	0/572
B	"	0/572	0/572	0/572
A	High	0/640	0/640	0/640
B	"	0/640	0/640	0/640

Table 3. Temperature Cycle (-65 to +150C) Reliability for Pad Type A and B.

Simulations of 5-Metal Layer BOA Pad Structures

Based on the stacking of the vias and contacts beneath the bond pad in Pad B, a higher incidence of functional failure was expected during assembly and package reliability testing. Due to the cost of designing and fabricating multilevel test wafers, mechanical simulations of the bonding pads were used to better understand the relative affects of pad structural elements. Therefore, models of the two pad types were developed and the stresses in the pad stack during wirebonding and during thermal cycling were simulated. The relative stresses were compared for different pad designs to determine how the placement of vias and metal in the bond pad affect the transfer of forces through the stack to the active silicon.

The multilevel copper/ SiO_2 pad structures were simulated using a 2-D axisymmetric model of the BOA pad stacks with the bonded ball center placed along the axis of symmetry. The forces applied to the bond pad were simulated by applying a static normal load to the top of the pad stack structure. A bonded ball diameter of 68µm was assumed for applying the static loading. Figure 6 depicts the model cross-sections with the applied wirebond loading. This model oversimplifies the forces that act on the pad during the wirebonding process. In reality, the forces are dynamic in both loading and direction and ultrasonic energy is applied the bond region by the transducer via the bonding capillary. In this simplified model, the effects of the ultrasonic energy input to the pad through the capillary and the thermal energy from the heated wirebonding stage are neglected.

The main concern in wirebonding over active devices is the degree to which the wirebond forces are transferred to the silicon-contact interface of the active silicon directly beneath the bond pad. The application of the static loading to the bond pad suggested that the maximum compressive stresses are applied around the periphery of the ball. Failure analysis in previous studies (2) showed that pad cratering initiated in the region beneath the edge of the bonded ball. Therefore, the areas of most interest in examining the silicon-contact interface stresses are regions below the vias and contacts and the region below the edge of the bonded ball.

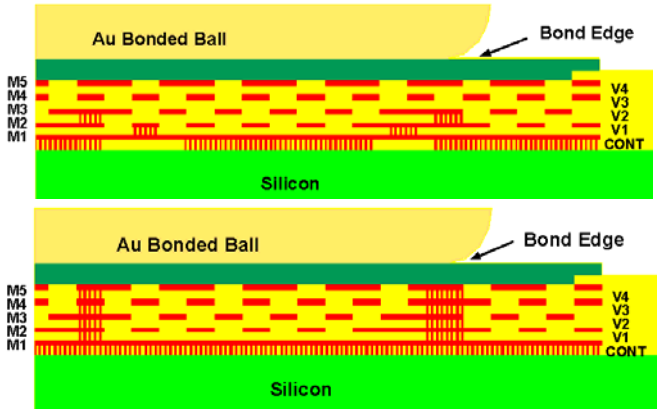

Figure 6. Model layouts for Wirebond Pads with BOA Types A (top) and Type B (bottom).

Principle and compressive stresses were evaluated by simulation to predict the areas in which active devices beneath the bond pad might be more at risk to damage during wirebonding. Two different failure mechanisms for the pad stack were anticipated based on the wirebond stresses.

The first failure mode investigated by simulation was dielectric cracking. Because the interlayer dielectric material is brittle, it will crack if the maximum principle stress in the ILD layers exceeds the dielectric materials fracture toughness. In the absence of fracture toughness data for the oxide dielectric material, the simulation results are used to compare the relative risks for the two pad stack types. Comparing the principle stress distributions for Pad Types A and B in Figure 7, little difference is noted in the maximum values or the stress contours. Therefore, dielectric cracking is not considered a higher risk in the Pad B structure. The maximum stress in the model occurred at the outer edge of the bonded ball, in the dielectric in the uppermost layer. The predicted location maximum stress appears to be in agreement with a previous study of Al/low-k pad structures [4] where cracks in the dielectric layer below the bond pad were found to initiate near the edge of the bonded ball.

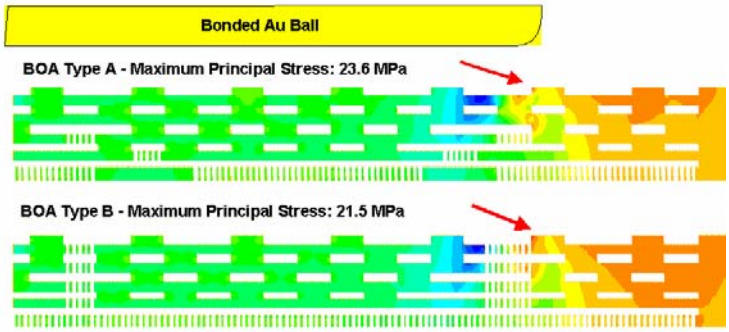

Figure 7. Predicted Principle Stresses (MPa) Simulated for Wirebonding on BOA Types A and B.

The second failure mode evaluated by simulation is that in which the compressive stresses are high enough at the silicon-to-contact interface that damage to the active device is possible, resulting in electrical failure. The simulation results again predicted the maximum stresses were located at the edge of the bonded ball and in the uppermost layers of the pad stack. Figure 8 shows more details of the compressive stress distribution in the pad structures below the edge of the bonded ball. The stresses developed at the M5/V4 interface and the contact/active silicon interface are plotted versus location. While the predicted maximum compressive stresses at the M5/V4 interface are 11% higher for Pad B, the maximum stresses at the contact-silicon interface are very nearly the same. In the regions of the pad stack where vias are not present and at the upper levels of the stack structure, the stress distributions are nearly identical. Therefore, the relative risk predicts for damaging the active silicon during wirebonding is no higher for the Pad B with stacked vias and contacts. The similarity of the stresses at the contact-silicon interface suggests that the affect of vias on the distribution of stresses is localized and that, given a few interposing metal layers between the bondpad and the silicon, the forces of wirebonding can be redistributed evenly before the contact layer.

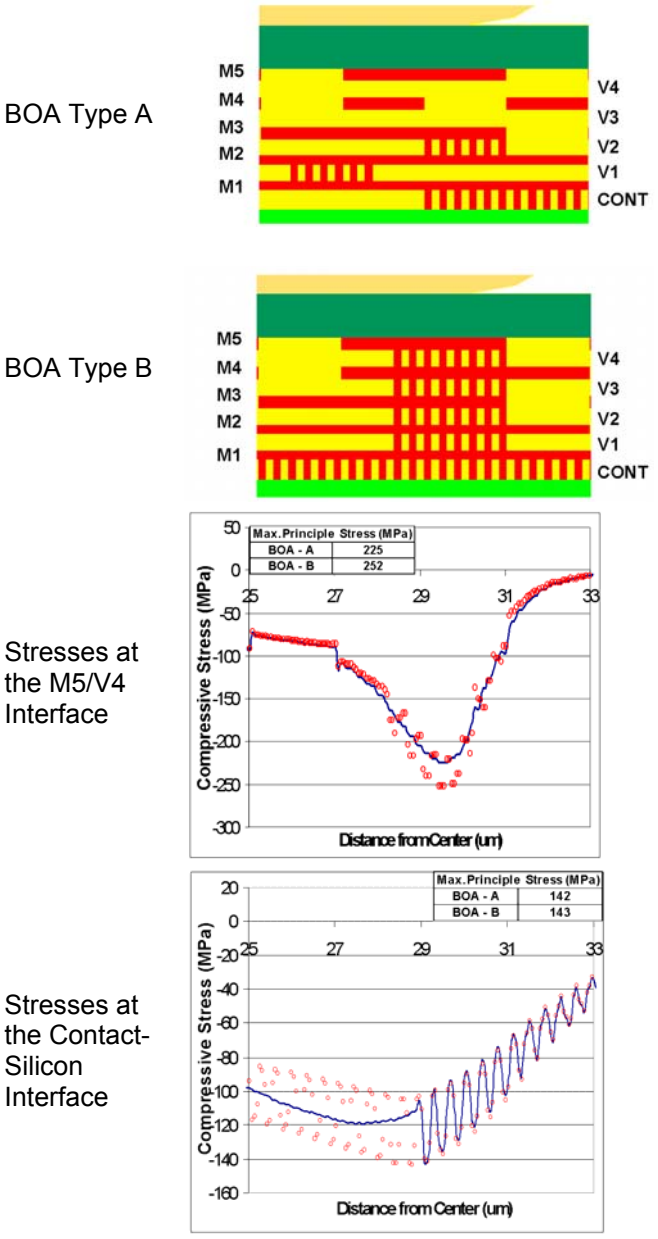

Figure 8. Compressive Stresses: M5/V4 and Contact/Si Interfaces: BOA-A (-, blue) and BOA-B (o, red)

The relative magnitude of stresses on the pad stack resulting from thermal cycling was also predicted by simulation. Since the bond pad stack is comprised of copper metal and dielectric material which have different coefficients of thermal expansion (CTE), temperature changes, such as those experienced during temperature cycling the packaged devices, induce stresses in the pad stack. A temperature change of +150°C to –65°C was simulated using the wirebonded pad stack to approximate the effect of package thermal cycling. Temperature-dependent nonlinear elastoplastic properties were used for the copper elements. The stress distributions developed are shown in Figure 9.

The maximum principle stresses were predicted to occur at the edges of the bond pad area in both BOA layouts. Very little difference in the stress distributions was predicted for the two BOA types. The placement of vias was not found to have an appreciable effect on the stress distribution. The result makes seems reasonable, since the material set is the same for both structures. However, the maximum principle stress predicted due to the CTE-mismatch is an order of magnitude greater than the maximum predicted during wirebonding. This suggests that localized dielectric cracking might be a concern in the region of the pad edge during thermal cycling.

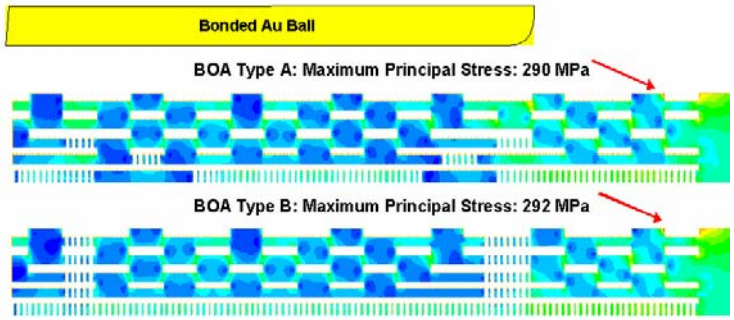

Figure 9. Comparison of Principle Stresses Developed in Temperature Cycle (–65°C to +150°C).

Conclusions and Recommendations

The placement of active circuitry in the excluded region beneath wirebond pads using *Bond Over Active* layout methods represents an effective method for reducing overall die size without sacrificing either assembly or package reliability. Two 5-metal layer, copper/SiO_2, test structures designed with different BOA layouts were compared using assembly and package reliability, and mechanical simulation. One pad structure included only a minimal density of active circuitry, with metal layers 1-3 utilized. The second BOA layout consisted of active metal at all five layers of the pad structure, with stacked vias connecting all of the metal layers and vias stacked over the contacts to active silicon. Both of these BOA layouts were evaluated using a standardized six-pad IO device.

The BOA test structures were assembled using both normal and high wirebond forces. Assembly reliability of both BOA types, determined by functional testing, was found to be excellent. . No failures were observed due to normal wirebonding forces. Only one of 1280 structures assembled with high wirebond forces yielded a continuity failure. Packaged device reliability in MSL3 preconditioning, autoclave stress (96 and 144 hrs), and temperature cycle stress (200, 500, and 1000 cycles) was also acceptable with no functional failures recorded at any of these readpoints. The lack of any difference in reliability between the two different BOA layouts was partially explained through a simplified mechanical simulation of the pad structures during wirebonding. The relative stress distributions at the contact-silicon interface suggested that vias only have a local effect on the distribution of stresses in the pad. This dissipation of the bonding forces was attributed to the comparable moduli of the copper metal and SiO_2 dielectric materials. The area of highest stress concentration was predicted to be in the uppermost layers of the pad structure near the edge of the

bonded ball. Mechanical damage disclosed in a previous study was found that supports this conclusion.

As wafer fab technologies advance and device speeds increase, low-K and ultra-low K dielectric materials will be incorporated into the back end flow. These materials have moduli that are 7-10 times lower than the current SiO_2 dielectric and may include fragile pore structures. The design of BOA pad structures in copper/low-k may present significant challenges. The design and evaluation of test structures with these low modulus dielectrics and the derivation of compatible BOA layouts is one area of focus for future work.

Acknowledgments

The authors would like to thank the following people for their support: Shailesh Mulgaonker for wafer processing and allocation; Sergio Ajuria for testing resources; Bill Williams for probe card design; Keith Bird and Rick Nolan for wafer probe and test program debug; Stan Cejka for package substrate design; Tim Thompson for final package testing; Roy Arldt for preparation of device cross-sections and SEM imaging; Julie Nadeau for package decap and SEM analysis.

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