ANALYSIS OF THE DATA STABILITY AND LEAKAGE POWER IN THE VARIOUS SRAM CELLS TOPOLOGIES

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Abstract

Due to CMOS technology scaling and the need of battery operated devices continues to drive the increase of on-die memory density to meet performance needs in various applications. Meanwhile, the device variation and leakage are increasing as the miniaturization of the transistor continues which also effects the realiability and performance of the device. As a result, it is increasingly challenging to develop SRAM with adequate stability margin for low-voltage operation while keeping the power consumption low enough to meet system-level power requirements.In this paper we analyse the performance of various toplogies of SRAM cells at various process technologies for enhancing the cell stability which is related to the cell SNM and the leakage power consumption.

Keywords:SNM,Cell Stability,Leakage Power, On-die Memory.

1. Introduction

In the past few years a tremendous rise in VLSI fabrication has led to incresed the densitites of integrated circuits by decreasing the device geometries.Such high density circuits support high design complexities and very high speed but susceptible to power consumption.Circuits with excessive power dissipation are more susceptible to run time failures and give rise to reliability problems [Chen, (2003)].

The other factors behind the low power deisgn is growing class of personal computing devices, e.g., as portable desktops,digital pens, audio and video based multimedia products and wireless communications such as PDA's and smart cards, etc.These deivces and systems demand high speed and complex design functionalities.The performance of these devices is limited by the size,weight and lifetime of portable battries. Memory design is an integral part in these devices and so reducing the power dissipation in these can improve the system power efficiency,performance,relaibility.

2. Conventional 6T SRAM Cell

SRAM have experienced a very rapid development of low power,low voltage memory design during recent years due to an increase demnad for notebooks,laptops,hand held communication devices and IC memory cards.Due to these concerns limiting power consumption is a must andhence new techniques are being realised to improve energy efficieny at all levels of the design.In this paper an overall analysis has been carried-out for the different SRAM cells at various technologies in respect to stability and leakage power consumption.

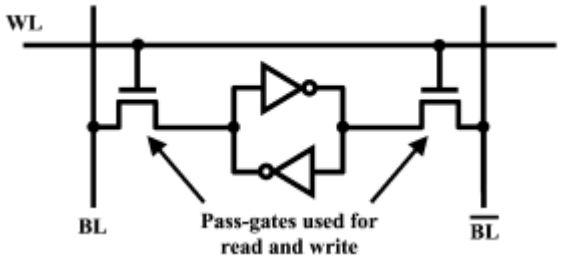

Fig.1 Conventional 6T SRAM Cell

In the traditional 6T-SRAM (Fig.1), the cells must be both stable (during a read event) and writeable (during a write event) ignoring redundancy; such functionality must be preserved for each cell under worst-case variation. At the cell level, transistor strength ratios must be chosen such that cell static noise margin and write margin are both maintained, which presents conflicting constraints on the cell transistor strengths. For the cell stability during a read operation, it is desirable to strengthen the storage inverters and weaken the pass-gates. The opposite is desired for cell write ability a weak storage inverter and strong pass-gates. This delicate balance of transistor strength ratios can be severely impacted by device variation, which dramatically degrades stability and write margins, especially in scaled technologies. Low supply voltages further exacerbate the problem as threshold voltage variation consumes a larger fraction of these voltage margins. Variability can thus limit the minimum operating voltage of SRAM [Singh, etal, (2008)].

To circumvent variability problems, many design techniques have been proposed to enable low-voltage operation of 6T cells. The addition of a second higher supply voltage dedicated to the SRAM array is an effective method to ensure sufficient margins with scaling of the logic supply voltage. In such a case, the SRAM voltage does not scale with technology and could even be increased as variability intensifies. Instead of being tied to a fixed higher supply, SRAM arrays could also use dynamically modulated supplies that are pulsed to different levels when a read or write event occurs. To an extent, this decouples read and write events from the standby condition such that the optimum bias conditions can be used in each case. Such techniques invariably add complexity to the design, but can be used to improve cell stability and write-ability or standby leakage. While tradeoffs between cell optimization for read and write can be reduced by these methods, they cannot be eliminated.

In a 6T cell, variability tolerance is compromised by the conflicting needs of cell read stability and write ability. Because the same pass-gate devices are used to both read and write the cell, it is inevitable that the two conditions cannot be simultaneously optimized. Just as dynamically modulated power supplies decouple requirements for read and write, such an effect can also be achieved by modifying the cell itself. The 6T SRAM cell stability problems also arise during a write operation to an unselected column when the word line is activated while both bit lines are held high. A situation that produces equivalent bias conditions to a read operation. So, different topologies of SRAM cell have been implemented at various technologies to improve the data stability and leakage power consumption [Chen, etal. (2008)].

3. Various SRAM Topologies at Different Technologies

(a).7T SRAM Cell

(i).At 90nm Technology

A read SNM free SRAM is implemented at 90nm technology using the techniques which are as given: first technique is that of increasing the Vth of the NMOS transistors in SRAM cells. Increasing the Vth of access NMOS transistors prevents Node V1 voltage from greatly exceeding “0”, while increasing the Vth of drive NMOS transistors increases the CMOS inverter logical threshold voltage. The second technique is that of dropping the word-line (WL) voltage level from VDD at Read operations [Takeda, etal. (2006)]. This has the same effect as

increasing the Vth of access NMOS transistors 64KB SRAM has been implemented at minimum Vdd of 440mv and 20 ns access time at 0.5 supply voltages Fig.2.

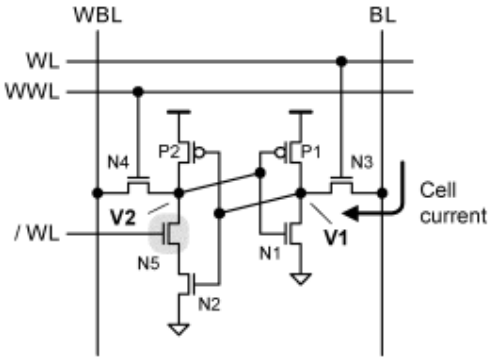

Fig.2 7T SRAM Cell

The limitation was write operations at lower Vdd cannot be performed and read operations at low Vdd levels result in low storage destructions in SRAM cells due to the leakage current of PMOS cells. The other 7TSRAM cell uses a novel write mechanism which depends only on one of the 2 bit-lines to perform a write operation, which reduces the activity factor of discharging the bit-line pair. The HSPICE simulation shows that the write power saving is at least 49%. Both read delay and static noise margin are maintained after carefully sizing the cell transistors.
The limitation was that area overhead from the conventional 6T SRAM cell [Aly, (2007)].

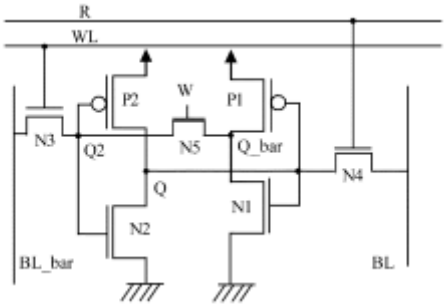

Fig.3 7T SRAM cell with Novel Write Mechanism

(b).8T SRAM cell

(i).At 90nm technology

A dual-port cell (8T-cell) is created by adding two data output transistors to a conventional 6T-cell, as shown in Fig. 4. Separation of data retention element and data output element means that there will be no correlation between the read SNM and Icell [Chung, etal. (2008)].

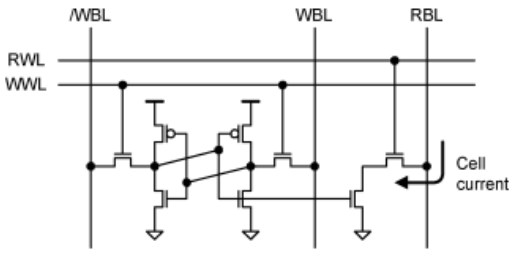

Fig.4 Dual-Port 8T SRAM Cell

In contrast to the worst normalized read SNM value of 0.20 for a conventional 6T-cell, here the value is 1.22, and there is no Icell degradation. It is also possible here to lower the Vth of the NMOS transistors in a SRAM cell in order to improve Icell. This 8T-cell has 30% more area than a conventional 6T-cell.The 30% area overhead is composed of not only the two added transistors but also of the contact area of the WWL, the word-line for write operations. While WL contact area is conventionally assigned to the boundary line between two SRAM cells, in this SRAM cell the WWL contact area is assigned to within a cell, as shown in Fig. 4 [Calhoun and Chandrakasan, (2007)].

(ii).At65nm Technology

An UDVS (Ultra dynamic voltage scaling) 8T SRAM Fig.5 is proposed in this read and write ports are decoupled,(BVSS) virtual ground node for read buffer and is kept at Vdd is cell is not accessed. Mchd is the virtual supply node & its voltage can be brought down during write access upto weaken PMOS.3 different write assist scheme used. A 64Kb SRAM fabricated with a die size of 1.4mm x 1mm.At 250 mv supply voltage, 20KHz frequency is obtained and at 1.2V, 200 MHz frequency is obtained. Low voltage operation is successfully achieved. RSNM problem is also resolved. The only limitation is the area overhead [Singangil, etal. (2009)].

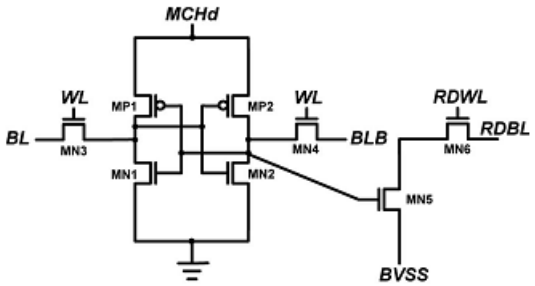

Fig.5 U-DVS 8T SRAM Cell

Another type of 8T SRAM cell with variability tolerance is proposed as shown in Fig.6. Two transistors as read stack are added with conventional 6T cell. Elimination of column select when the 8T array is floor planned, so that all the bits are spatially adjacent. The proposed 32 kb sub array operates at 5.3 GHz at 1.2 V & 295 MHz at 0.41V [Chang, etal. (2008)].

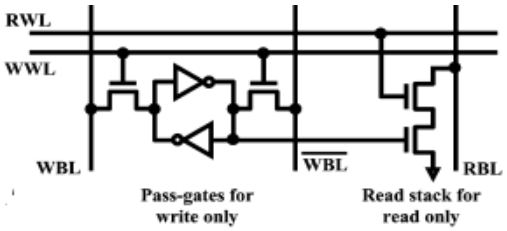

Fig.6A 8T SRAM Cell with Variability Tolerance

It has the following achievements,
(1).Improves variability tolerance due to the process variation, temperature and voltage
(2).Low voltage operation
(3).High Speed Operation SRAM caches
(4).Leakage reduction when Vdd is scaled from 1.2V to 0.41V
(5).SNM Improvement

But it has the limitation of the design complexity and area overhead.

An 8T subthreshold SRAM proposed in Fig.7, with sense amplifier has been proposed. It has "Zero" leakage read buffer, to resolve read buffer footer limitation charge pump circuit is used; BFB node gets bootstrapped to approximately 2Vdd.

virtual supply which is used Vdd for internal feedback control. It uses Sense amplifier redundancy concept [Verma and Chandrakasan (2008)].

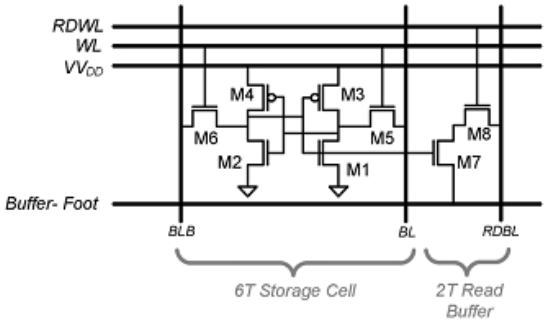

Fig.7An 8T Subthreshold SRAM

It has the following features,

(1).High density SRAM uses an 8 T cell
(2).Minimum operating voltage is 350mv
(3).Cell stability is also taken care off
(4).At its lowest operating voltage, the entire 256 kb SRAM consumes 2.2 µW in leakage
(5).Buffered read is used to ensure read stability

The constraint with this design is that speed decreases as the maximum operating is25KHz.

(iii).At 45 nm technology

The conventional dual-port SRAM cell comprised of eight transistors (8T SRAM) is shown in Fig.8. The 8T SRAM frees a static noise margin (SNM) in a read operation because it has a separated read port. Meanwhile, a precharge circuit must be implemented on a read bitline (RBL) so that the two NMOS transistors at the read port can sink a bitline charge to the ground. Thus, a certain amount power is dissipated by pre-charging. In addition to the precharge circuit, we have to prepare a bitline keeper on the RBL which imparts negative influence on a readout time. To make the matters worse, the delay overhead becomes larger as a supply voltage (VDD) decreases because of the bitline keeper [Noguchi, etal. (2008)].

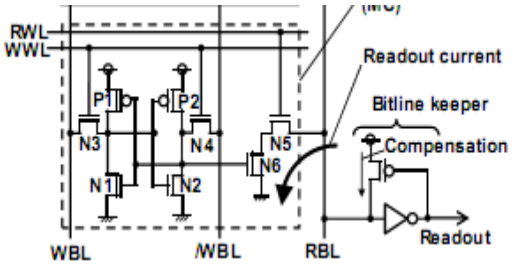

Fig.8A Dual Port 8T SRAM Cell

(c).9T SRAM Cell

(i).At65nm technology.

A new 9T SRAM cell as shown in the Fig.9 is proposed for simultaneously reducing leakage power and enhancing data stability. The proposed 9T SRAM cell completely isolates the data from the bit lines during a read operation. The read static-noise-margin of the proposed circuit is thereby enhanced by2 as compared to a conventional six-transistor (6T) SRAM cell. The idle9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption by 22.9%as compared to the standard 6T SRAM cells in a 65-nm CMOS technology.

The leakage power reduction and read stability enhancement provided with the new circuit technique are also verified under process parameter variations [Keerthi and Geens (2008)].

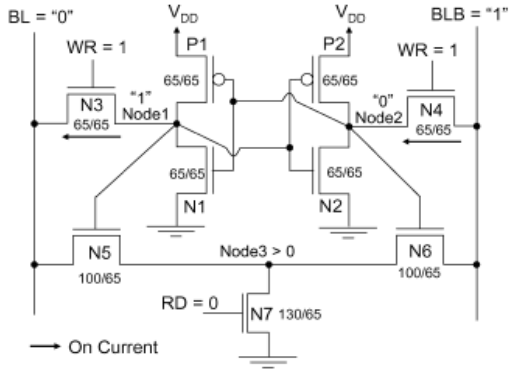

Fig.9 A 9T SRAM cell

(d).10T SRAM Cell

(i).At 65 nm technology

The dual Port SRAM (10T) as shown in the fig has only one read or write can occur per cycle, able to operate the SRAM in subthreshold region Fig.10.

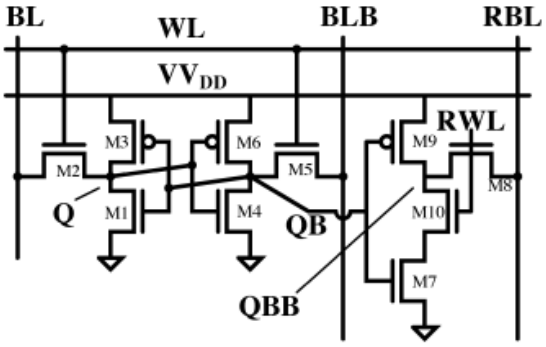

Fig.10 A 10T SRAM Cell

It has the following features,

(1).Substantial power savings and operates below 400mv
(2). 10T SRAM can remove the problem of read SNM by buffering the stored data during a read access
(3). It has 16% less leakage than conventional 6T SRAM
(4).Read SNM and WM also improved

Here the major limitation is that it is area inefficient and power saving is at the cost of speed.

(ii).At 45 nm Technology

At 45 nm a 10T Single End SRAM (10T-S SRAM) is proposed which is non-precharged SRAM with a single-end read bitline as depicted in Fig.11 (hereafter, we call "10T-S SRAM"). Two PMOS transistors are appended to the 8T SRAM cell, which results in the combination of the 6T conventional cell, an inverter and transmission gate. The additional signal (/RWL) is an inversion signal of a read wordline (RWL); it controls the additional PMOS transistor (P4) at the transmission gate [Taufik and Kursun, (208)].

While the RWL and /RWL are asserted and the transmission gate is on, a stored node is connected to an RBL through the inverter. It is not necessary to prepare a precharge circuit because the inverter fully charges/discharges the RBL. The 10T-S SRAM is having the lowest power. This is because the transition possibility of the RBL is 50% when a sequence of random data is considered.

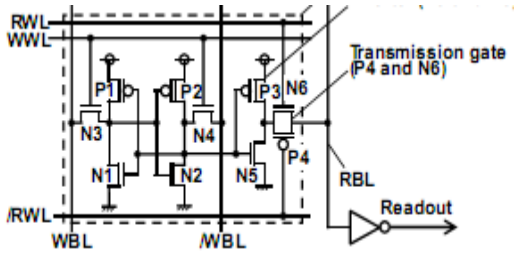

Fig.11 A 10T Single End SRAM (10T-S SRAM)

Another type of 10T SRAM is as shown in Fig11 shows a schematic of a 10T SRAM with differential read bitlines (RBL and /RBL). Two NMOS transistors (N5 and N7) for the RBL and the other additional NMOS transistors (N6 and N8) for /RBL are appended to the conventional 6T SRAM. As well as the 8T SRAM, precharge circuits must be implemented on the RBL and /RBL [Taufik and Kursun, (208)].

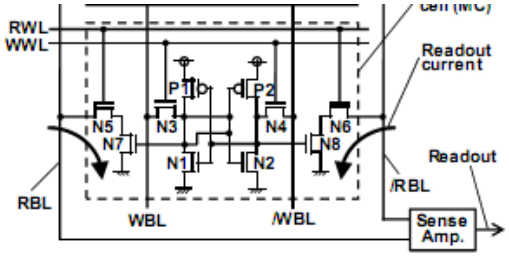

Fig.12 A 10T Differential SRAM (10T-D SRAM)

On the other hand, in the 10T-D SRAM, the average voltage difference between the RBL and /RBL is 80% of VDD (0.8V) as mentioned in the previous subsection, even if the sense point in the worst-case is set to 50 mv.It can operate fast at 1V and 755MHz.

(e).11T SRAM

(i).At 65nm Technology

In Fig.13 the schematic of the 11T-SRAM bitcell is shown. Transistors M2, M4, M5, and M6 are identical to 6T-SRAM, but two transistors M1 and M3 are downsized to the same size as the PMOS transistors.

The bitline and wordline are distinct from the write wordline. In this case, memory can have distinct read and write ports. During the hold time, RDWL and WL are not selected. Minimum size transistors were used for the added 5T-circuitry, except the access transistor that has a larger size. The most important part of the 11T-SRAM is a boost capacitor (CB) that connects source of M9 to RDWL [Moradi (2008)].

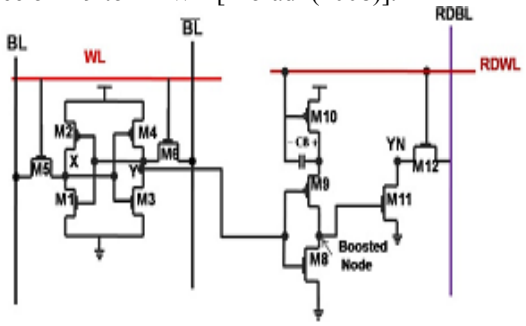

Fig.13 An11T SRAM Cell

Hence, supply voltage is kept more than 0.3V. In this case, both the cell is runningat a satisfactory speed with a proper write noise margin. The effective area overhead for the proposed circuit is typically between 22% to 28%, but due to the employment of minimum size devices and lowering the sizes of PMOS devices in 6T-SRAM and also downsizing the NMOS transistors in 6T-SRAM cell, the area overhead may be reduced. The SNM is significantly increased (more than 6X in some cases compared with 6T-SRAM) .

Conclusion

In this paper various SRAM cell topologies which are designed for low power applications along with the stability has been discussed and they are discussed at various proves technologies as process variations is now –a- days a prime concern in realizing the performance of a circuit. It gives a road map how the various SRAM circuits are being designed stating the various features with their limitations.

Acknowledgment

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