A BIST (BUILT-IN SELF-TEST) STRATEGY FOR MIXED-SIGNAL INTEGRATED CIRCUITS

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Munich, 2004

Abstract

BIST (Built-in Self-Test) Strategy for Mixed-Signal Integrated Circuits

Recently, more and more system functionalities have been integrated onto a single chip, because the electronic systems become more complex and the very deep sub-micron technologies make such an integration possible as well. Consequently, mixed-signal ICs (Integrated Circuits) which combine both digital and analog parts on the same substrate are widely employed. But the high density, limited I/O pins, and especially, the analog nature of such ICs make their testing both difficult and expensive. In all the proposed test methods, DFT (Design for Test) and BIST (Built-In Self-Test) techniques have been proven to be very effective by the meaning of increasing the observability and controllability of the CUT (Circuit under Test).

This work presents DFT and BIST techniques for the production testing of mixed-signal circuits. The special test strategies for the typical mixed-signal components ADC (Analog-to-Digital Converter) and DAC (Digital-to-Analog Converter) implemented on one chip are discussed. The traditional test for such mixed-signal components can be completed through a DSP-based mixed-signal tester with an arbitrary waveform generator and a signal digitizer. But such a test is very costly and time-consuming. Hence a BIST strategy based on a loop structure is proposed in this work for testing ADC/DAC pairs. This BIST method is called Loop-BIST and takes the advantage of the presence of the ADC and the DAC on the same chip: the analog parts of the ADC to be tested and the DAC to be tested are connected together to form a fully digital loop so that the loop test is a digital driven one. In such a way, the test can be moved from the mixed-signal domain to the digital domain which is much easier and more cost-effective. According to the different resolution of the ADC or the DAC, the loop and the sequence of the testing steps should be different as well. All these issues are discussed in this work along with some industrial application cases.

This BIST method realizes the test control, test stimulus generation and test response evaluation at the aspect of the on-chip circuitry. Various methods for generating a test stimulus and for evaluating a test response are discussed in this work. These methods can be also employed for other BIST applications. In this work, a new digital scheme based on filtering a periodical signal finds its application in the generation of a digital stimulus. Meanwhile the DELTA-SIGMA modulation technique is used as a generation method for an analog stimulus. The dynamic parameters can be extracted through

a notch filter, without needing the presence of an on-chip DSP. This makes the proposed BIST approach more common. Moreover, a new DAC BIST method is given, which is based on the one-point-multi-level algorithm. In designing and implementing the BIST scheme, a particular filter type – a WDF (Wave Digital Filter) is involved. This class of filter has been known for several years. Its economic realization and low coefficient sensitivity have made it a design technique exploited in many low-power, up-to-date applications. The demonstration of the proposed Loop-BIST is given through various simulation results in the last parts of this work.

Zusammenfassung

BIST (Built-in Self-Test) Strategie für integrierte Mixed-Signal Schaltungen

Die steigende Komplexität elektronischer Systeme führt heute dazu, mehr und mehr Systemfunktionalitäten auf einem einzigen Chip integrieren zu wollen. Neue Technologien, wie die sogenannten Deep-Submicron-Technologien, machen es möglich solche ehrgeizigen Ziele auch in die Realität umsetzen zu können und die gemeinsame Integration von digitalen und analogen Schaltungen auf dem gleichen Substrat voranzutreiben. Die entstehenden hohen Integrationsdichten, die damit verbundenen begrenzten Möglichkeiten der Zugänge zu inneren Schaltungsknoten und insbesondere das analoge Verhalten solcher gemischter integrierter Schaltungen machen die abschließende Qualitätsüberprüfung, den Vorgang des Testens, sehr schwierig und teuer. Akzeptierte Methoden, welche den Test oder die den Test unterstützenden Maßnahmen bereits im Design berücksichtigen bzw. implementieren (DFT: Design For Test) oder welche sogar sich selber testende Schaltungen ins Design einbetten (BIST: Built-In Self-Test), haben schon ihre Effektivität im Hinblick auf erweiterte Beobachtbarkeit und Steuerbarkeit der zu testenden Schaltungen gezeigt.

Die vorliegende Arbeit untersucht DFT- und BIST-Techniken für den Produktionstest von gemischten analogen und digitalen integrierten Schaltungen (Mixed-Signal-Schaltungen). Es werden verschiedene Teststrategien für typische Mixed-Signal-Anwendungen diskutiert, die sowohl einen Analog-Digital-Converter (ADC) als auch einen Digital-Analog-Converter (DAC) auf einem Chip integrieren. Der traditionelle Testflow für solche Mixed-Signal-Komponenten wird auf ein DSP-basiertes Mixed-signal-Testsystem zurückgeführt, das einen allgemeinen Signalgenerator (Wave Form Generator) und einen Digitalisierer (Signal Digitizer) verwendet. Der Nachteil solcher automatisierter allgemein verwendbarer Testsysteme liegt jedoch in ihrem hohen Zeit- und Kostenaufwand. Daher wird in dieser Arbeit für Tests, die auf das Pärchen ADC und DAC zurückgreifen können, eine Teststrategie vorgeschlagen, welche auf einer rückgeführten Schleifenstruktur basiert. Diese BIST-Methode ist in der Literatur als Loop-Back BIST bekannt und hat den Vorteil, dass ADC und DAC, die ja beide auf einem Chip vorhanden sind, für den Test verwendet werden können. Die zu testenden analogen Teile von ADC und DAC werden so kombiniert, dass eine rein digitale Schaltung entsteht, um dann einen digital getriebenen Schaltungstest durchführen zu können. Der Mixed-Signal-Test wird so zum Digital-Test umgewandelt, was für viele Anwendungen einfacher und kostengünstiger ist. Je nachdem, ob die Auflösung von ADC oder DAC unterschiedlich ist, wird die Schaltung und dementsprechend die Rei-

henfolge der Tests geändert. Alle oben genannten Methoden werden in dieser Arbeit an Hand von Beispielen aus industriellen Anwendungen beschrieben.

Die vorgestellte BIST-Methode realisiert ihre Steuerung, Signalerzeugung und Signalauswertung in Hinblick auf eine Implementierung auf einem gemeinsamen Chip. In dieser Arbeit werden verschiedene Simulations- und Auswertemethoden vorgestellt, die auch ihre Anwendung in BIST-Applikationen gefunden haben. Ein neues digitales Schema, das periodische Signale durch Tiefpassfilterung erzeugt, wird für die Erzeugung von digitalen Signalen untersucht. Mittlerweile wird die DELTA-SIGMA-Modulationstechnik zur Erzeugung von analogen Signalen verwendet. Dynamische Parameter können durch Sperrfilterung, ohne Unterstützung eines DSP, extrahiert werden. Zusätzlich wird eine DAC-BIST-Methode vorgestellt, die auf dem „One-Point-Multi-Level"-Algorithmus basiert. Das Wave Digital Filter wird hierbei für Design und Implementierung des BIST-Schemas vorgeschlagen und implementiert. Im letzten Kapitel wird die vorgeschlagene Loop-Back BIST-Methodik durch Simulationsergebnisse validiert.

Contents

Chapter 1

Introduction

1.1 Motivation

Due to the increasing complexity of electronic systems and the capabilities of very deep sub-micron technologies, more and more system functionalities have been integrated onto a single chip in recent years. Consequently an increasing number of chips that combine digital and analog functions are designed. High-performance applications of mixed-signal Integrated Circuit (IC) in many areas such as wireless telecommunications, data exchange systems and satellite communications have greatly increased. This development drives test equipments towards a single platform solution that can test both digital and analog structures on a single chip. On the one hand, by mixed-signal test equipments, the digital requirements are equivalent to those for purely digital chips. On the other hand, mixed-signal Automated Test Equipments (ATE) must be modular and expandable. Consequently, they must across the entire spectrum from digital-only to the full integration of high performance analog/RF/microwave instruments, which leads to the high cost of the mixed-signal ATEs. Traditionally, ATE's cost is measured using a simple cost-per-digital pin approach. But such calculation ignores not only base system costs associated with equipment infrastructure and central instruments but also the beneficial scaling that occurs with increasing pin count. Therefore, it is suggested to present and evaluate the ATE's cost roadmap by the following equation [4]:

$$TC = b + \sum (m\,x) \tag{1.1}$$

In this equation TC is the cost of testers, b is the base cost of a test system with zero pins; m is the incremental cost per pin; x is number of pins. Note that b scales with capability, performance, and features, while m depends on memory depth, features, and

analog capability. The base cost *b* varies by the different tester segment. The summation addresses mixed configuration systems that provide different test pin capability (i.e., analog, RF, etc.). The costs for factor *b* and *m* are expected to decrease over time for equivalent performance points. The typical values of *b*, *m* and *x* for different testers are given in Table 1.1 [4].

Table 1.1: ATE cost parameters [4]

Tester Segments	b	m	x
	Base Cost	Incremental Cost per Pin	Pin Count
	k$	$	
High-performance ASIC	250-400	2700-6000	512
Low-end ASIC	200-350	1200-2500	256-1024
Mixed-signal	250-350	3000-18000	128-192
Memory	200+	800-1000	1024
RF	200+	~50000	32

From this table, it can be seen that the price of a typical ATE (esp. a typical mixed-signal tester) is very high. A roadmap about the development for the mixed-signal tester is available in Appendix A. Nevertheless, the ATE cost is one of the most expensive elements of the overall manufacturing test cost that includes the cost of associated manufacturing cell equipment, materials, labor, floor space, equipment support, and manufacturing cell efficiency. Although some efforts have been made to decrease the percentage of the ATE cost among the overall cost, such as the combination of equipment cost improvement and reduction in equipment capability requirements, increasing the use of parallel test and reducing device test time and so on, the relative high cost of analog/mixed-signal testing instruments and the length of test time associated with testing remain the key challenges. For products in some market segments, test may account for more than 70% of the total manufacturing cost. Moreover, test cost does not directly scale with transistor count, die size, device pin count and process technology, which is illustrated in Fig. 1.1 [77].

Moreover, testing a mixed-signal circuit is still a difficult and challenging task since it must ensure the full functionality, quality and performance criteria for each functional

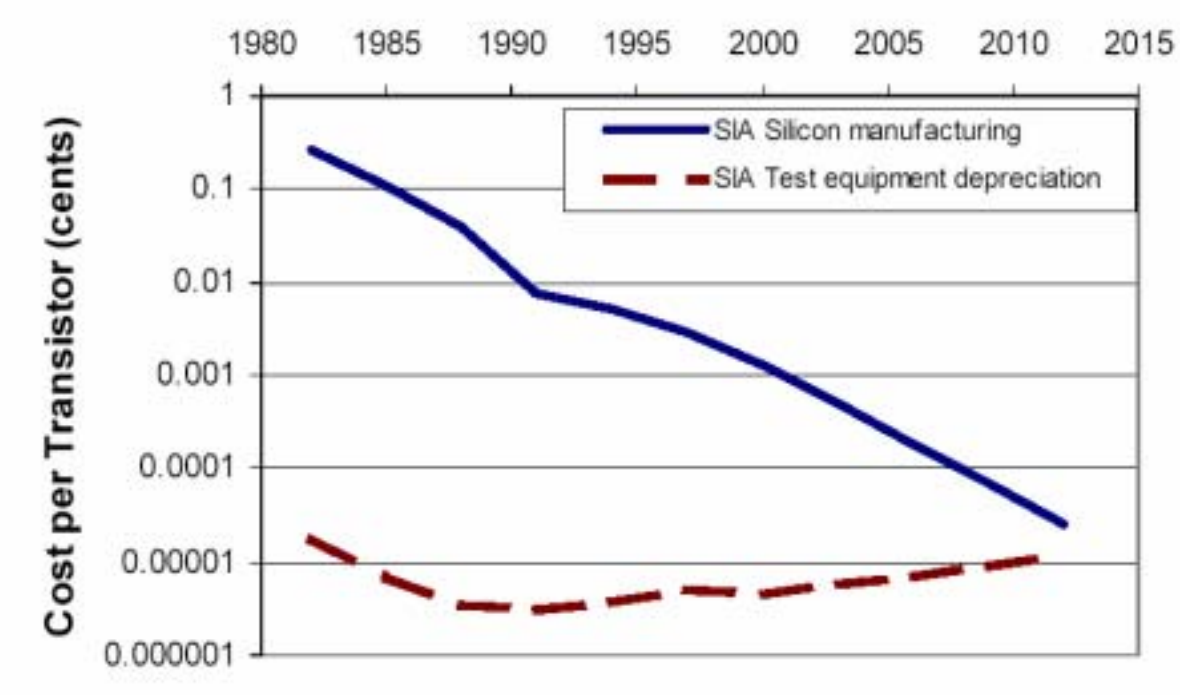

Fig. 1.1: Test cost vs. manufacturing cost (From Semiconductor Industry Association) [77]

block and for system-level operation. Analog circuits are often non-linear, include noise and have parameters that vary widely. The relationship between input and output signals in analog circuits is difficult to model. This limits the ability to develop effective, accurate and generally applicable fault simulation and test generation algorithms. Complex analog circuits can also be considered as mixed-signal circuits, since they generally employ logic and signal switching circuits to control and configure their operation. Mostly, in a mixed-signal circuit, the digital part often occupies much greater area than the analog part. However, the analog part often accounts for most of the overall test cost and time [1] [2] [5], which is illustrated in Table 1.2.

Table 1.2: Unproportionate testing cost for the analog part [5]

Mixed-signal IC	Digital Part	Analog Part
Area	80-90 %	10-20 %
Design Effort	20 %	80%
Test Cost	15%	85%
Added Value	10%	90%

Many papers [1] [2] [3] have discussed the testing factors which contribute to the analog test complexity, and such factors are summarized as follows:

- The analog circuits are very sensitive to environmental variables, which makes

their responses susceptible to many factors, such as the variations in the component values, the noise and thermal effects, etc.

- It is much more difficult to locate the defects on the analog circuits than that on the digital circuits because of the continuous nature of time and voltage of the analog operation.

- Due to the non-linearity of the analog systems, their performances depend heavily on circuit parameters. Even process variations within acceptable limits can also cause great performance degradation.

- The testing accuracy of the mixed-signal systems depends heavily on the resolution of test equipment and the accuracy of input testing stimuli.

- In digital circuits, the relationship between input and output signals is Boolean in nature. In the case of analog circuits, the input-output relationship is non-Boolean, complex and difficult to model.

- It is much more complicated and difficult to model the input-output relationship in analog circuits. So the extraction of the fault model of mixed-signal systems is a huge and hard task, which makes the testing simulation based on the fault model more difficult. Therefore, the simulation results are also questionable and not so convincing.

- The digital DFT schemes based on the structural division of circuits are usually no longer available when applied to analog circuits because of their great impact on the circuit performance.

- Analog functional tests are usually costly and time-consuming, because different specifications are seldom able to be tested in the same manner. The different manners mean more test programming efforts and, in most cases, extra efforts for hardware design. Moreover, limited functional verification often does not ensure a defect-free testing.

- Large safety design margins into digital circuits are considered. In analog circuits due to tight design margins, process variations within allowable limits can cause unacceptable performance degradation.

In addition, compared with the analog test, the test for mixed-signal circuits has even more problems because both analog and digital circuits are built on the same substrate

and they might be disturbed not only by the internal influence but also by the external influence. For example, the noise from the digital parts may produce the unwanted influence on the function of the analog parts.

Since there are so many problems present by the traditional test for mixed-signal circuits, as an alternative, the mixed-signal Built-In Self-Test (BIST) technique (or Design for Test: DFT) is becoming more and more important in the production test. It enables each element in a mixed-signal chain to be tested independently. This reduces the requirement for complex functional tests and improves test reuse. What's more important is that the BIST technique can reduce the production cost through building test circuitry on chip and that it can also check long term reliability through periodic self-testing of the chip performance. Generally speaking, BIST has the following advantages: 1) costly external test equipment can be eliminated, 2) parasitic effects introduced by cables connecting the equipment to the device are avoided, 3) testing speed technology is kept up-to-date with newer-generation integrated circuits, 4) reduction of test time through parallelization, 5) analog multiplexes to make the internal nodes accessible do not need to be included in the design, 6) mere manufacturing tests can be extended towards on-field diagnoses: a self-testable device can be examined from a remote location, and 7) checking long term reliability through periodic self-testing of chip performance.

Therefore, the motivation of this Ph. D work is to explore a BIST method for the test of the mixed-signal circuits, and, especially, to present a BIST approach for typical mixed-signal circuits, so-called ADCs and DACs. Since ADCs and DACs are often used in pairs, the BIST approach for testing the ADC/DAC pairs will be discussed thoroughly in this work.

1.2 Contributions

The following key issues and contributions in analog/mixed-signal BIST are addressed in this dissertation:

1. A new test technique oriented to production test of the embedded ADC/DAC pairs in mixed-signal ICs.

    a. Complex analog components on the analog signal path are not necessary.

   b. The impact of the test circuitry in the circuit performance is negligible.

2. A new BIST approach for the SNR testing of the DAC on chip, which uses a sinusoidal signal as the input stimulus and a notch-filter as the response analyzer. It presents some considerable advantages with respect to other previous work such as:

   a. The extraction of the dynamic character of the Circuit under Test (CUT).

   b. The further extraction of the static character of the CUT.

   c. High controllability is achieved for test stimulus application due to the fully digital generation method.

3. A new approach for on-chip sinusoidal signal generation embedded into mixed-signal circuits, which is based on the Fourier theory.

4. Improvements to the present notch filter method for the SNR extraction.

5. A new Signal-to-Noise Ratio (SNR) extraction method, which can be applied into BIST, when only little resources are available on chip.

6. The research on the application limitations of the notch filter for BIST.

7. The first summary of BIST methods for the ADC/DAC pairs.

1.3 Overview

In order to illustrate the contents of this research, an overview of this dissertation is shown in Fig. 1.2. The work is organized in the following form:

After an introduction of this dissertation in Chapter 1, the basic structures of the mixed-signal circuits are introduced in Chapter 2, by which the testing of the ADCs and DACs is introduced as well. In this chapter, the static and dynamic characteristics of the converters are addressed. The basic issues in analog and mixed-signal testing as well as some previous work about BIST techniques are reviewed in this chapter.

The purpose of Chapter 3 is to describe a common rule for the BIST design for the ADC/DAC pair testing, which is called Loop-BIST. In this chapter, three different cases are concentrated according to the different relationship between the DAC's resolution and the ADC's resolution.

Chapter 4 deals with a particular class of filter, the so-called wave digital filter, with the purpose of introducing its outstanding characteristics such as economic realization and low coefficient sensitivity.

In Chapter 5, the design of a new approach for on-chip sinusoidal signal generation is proposed after the description of alternative generation methods. Similarly, a fully digital approach for measuring the testing response with a digital notch filter is addressed and compared with other methods in Chapter 6.

Then, the implementation and the simulation results of the Loop BIST are given in Chapter 7. A new BIST approach for the Signal-to-Noise Ratio (SNR) testing of the DAC on chip, which uses a sinusoidal waveform as the input stimulus and a digital notch filter for response measurements, is also presented in this chapter. Lastly, the conclusion and the future work are presented in Chapter 8.

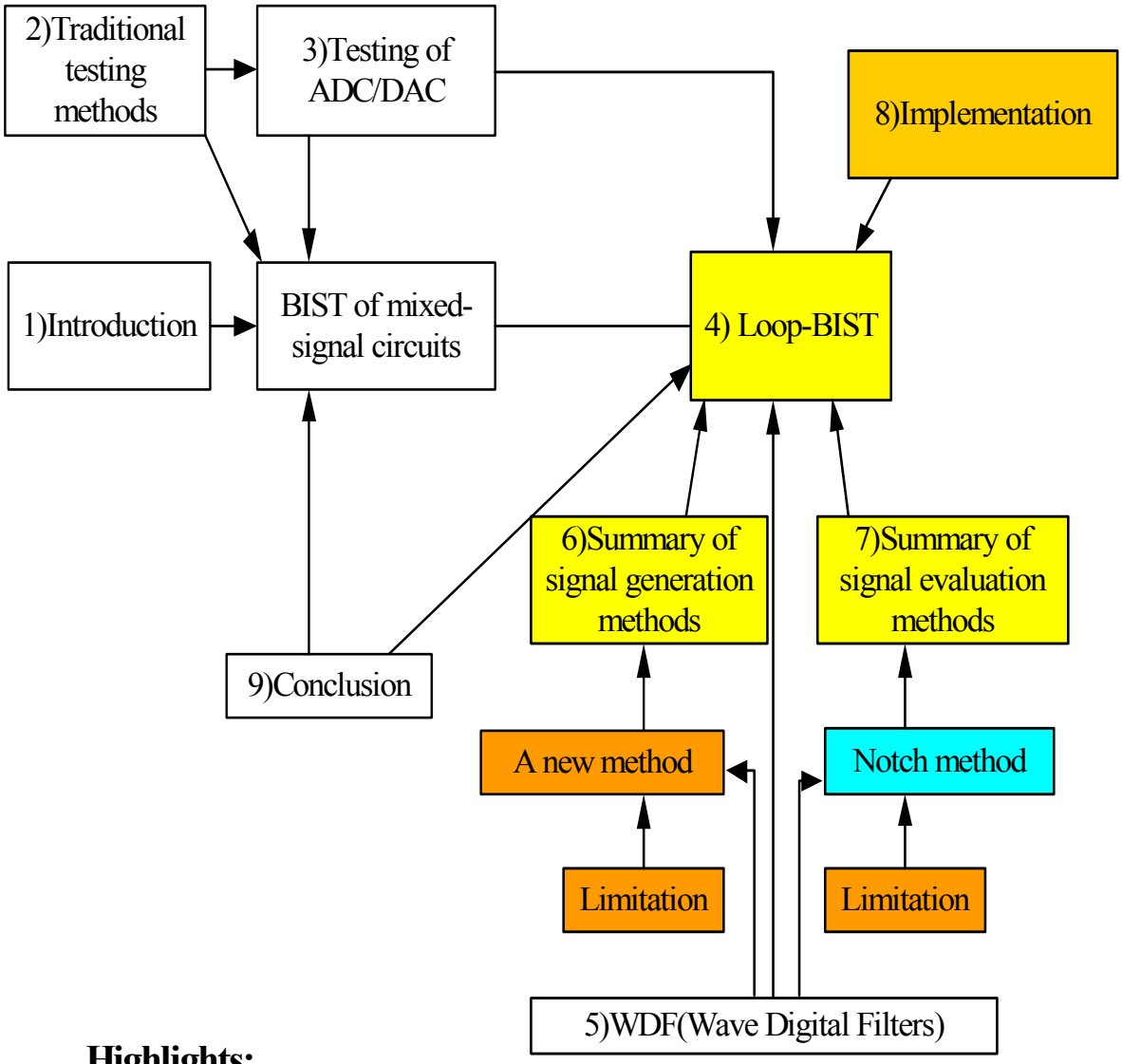

Fig. 1.2: The structure of the dissertation

Chapter 2

The Testing of ADC and DAC

In this chapter, the testing of two typical mixed-signals circuits – analog-to-digital converter (ADC) and digital-to-analog converter (DAC) – is presented. It will be shown which parameters of the converters should be extracted through the test and what a typical mixed-signal testing environment it is. Finally, an introduction about the efforts in the research of BIST methods for the ADC and DAC testing will be given.

2.1 Testing of ADC

ADC provides the link between the analog world and digital systems. There are lots of books (or papers) about the principle, performance, architecture and design of ADCs employed in high performance systems. The detailed information about the ADC principles as well as its architectures can be found in [35]. In the following, a brief introduction about the testing topics of the ADC will be given.

An ADC is a component that converts the analog input to its corresponding digital value. In other words, it can produce a digital output denoted by D as a function of the analog input denoted by A:

$$D = f(A) \tag{2.1}$$

Due to the infinite input, the output is chosen from a finite set of digital word lengths, which means that the ADC approximates each input level with one of these codes. Such approximation or rounding effect by AD operation is called quantization and the difference between the original analog input and the digitized output through quantiza-

tion is represented as quantization error. Fig. 2.1 depicts a simple ADC in-out characteristic and the corresponding quantization error. Note that the minimum change in the input that causes a change in the output is Vref/(2^m –1) (Vref is the input full scale voltage and *m* is the bit number of the output) and corresponds to the Least Significant Bit (LSB).

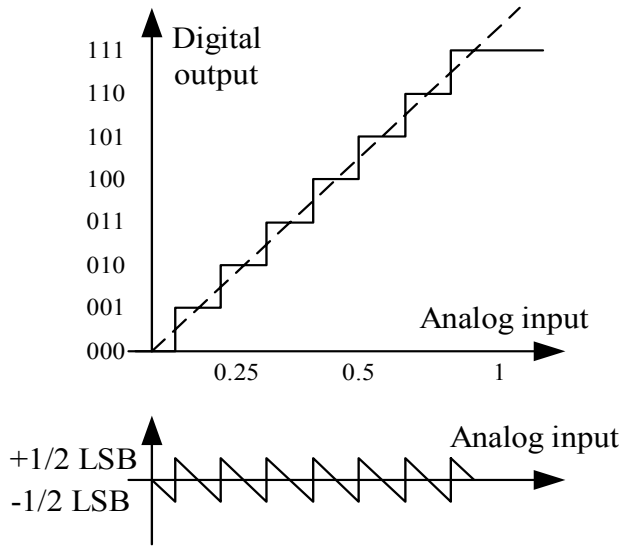

Fig. 2.1: Function of ADC and quantization error

Since an ADC is a mixed-signal component, there are many noise sources inside the converter due to its analog nature, which leads normally to that the characteristic of the ADC is not an ideal one. Fig. 2.2 shows a non-ideal ADC. The following definitions describe the static behavior of an ADC:

- Differential nonlinearity (DNL) is the maximum deviation in the difference between two neighbor code transition points on the input axis from the ideal value of 1 LSB.

- Integral nonlinearity (INL) is the maximum deviation of the input/output characteristic from a straight line passing through its end points (line AB in Fig. 2.2). The overall difference plot is called the INL profile.

- Offset is the vertical intercept of the straight line through the end points.

- Gain error is the deviation of the slope of line AB from its ideal value (usually unity).

Often specified as a function of the sampling and input frequencies, the following

terms are used to characterize the dynamic performance of converters.

- Signal-to-noise ratio (SNR) is the ratio of the signal power to the total noise power at the output (usually measured for a sinusoidal input). By the sinusoidal input the relationship between the SNR and the resolution of the ADC can be addressed by:

$$SNR\ [dB] = 6.02m + 1.76 \tag{2.2}$$

- Signal-to-Noise-and-Distortion Ratio (SNDR) is the ratio of the signal power to the total noise harmonic power at the output (usually measured for a sinusoidal input).

- Effective Number of Bits (ENOB) is defined by the following equation:

$$ENOB = \frac{SNDR_p - 1.76}{6.02} \tag{2.3}$$

where $SNDR_p$ is the peak *SNDR* value of the converter expressed in decibels.

- Dynamic range is the ratio of the power of a full-scale sinusoidal input to the power of a sinusoidal input for which $SNR = 0$ dB.

It is important to note that only some frequently used metrics are listed in this work.

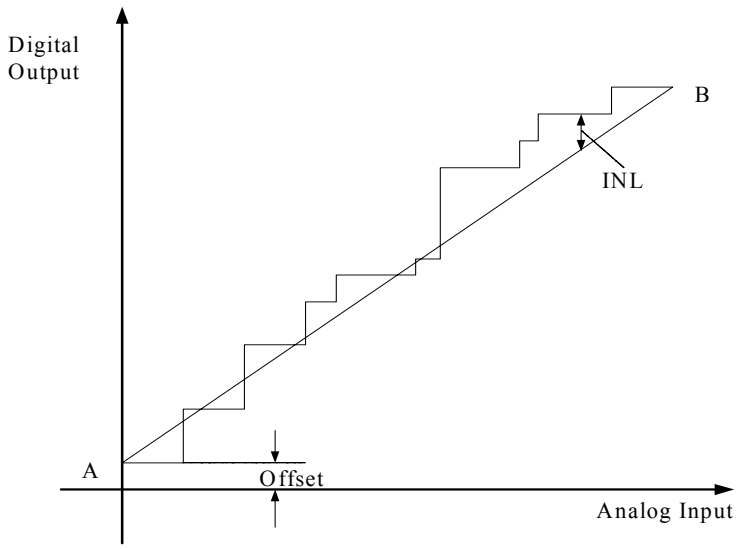

Fig. 2.2: The characteristic of a non-ideal ADC

For a complete set of specifications please refer to [35] and the other data books from different manufacturers.

2.2 Testing of DAC

DACs play a great role in the mixed-signal world because they are not only the bridge between the digital circuit and the analog domain but also the inter-stage in many multi-step ADCs, which reconstructs the analog estimates of the input. The relationship between the input and output of a DAC can be described by:

$$A = g\ D \tag{2.4}$$

where A is the analog output, D is the digital input, and g is a proportionality factor. For an ideal DAC the analog output level follows a straight line passing through the origin and the full-scale point which is illustrated in Fig. 2.3. The characteristic of a non-ideal DAC is illustrated in Fig. 2.4. Some terms usually used to characterize DA converters will be introduced. A complete set of specifications can be found in [35] [36] and the data books from different manufacturers.

- Differential nonlinearity (DNL) is the maximum deviation in the output step size from the ideal value of one Least Significant Bit (LSB).

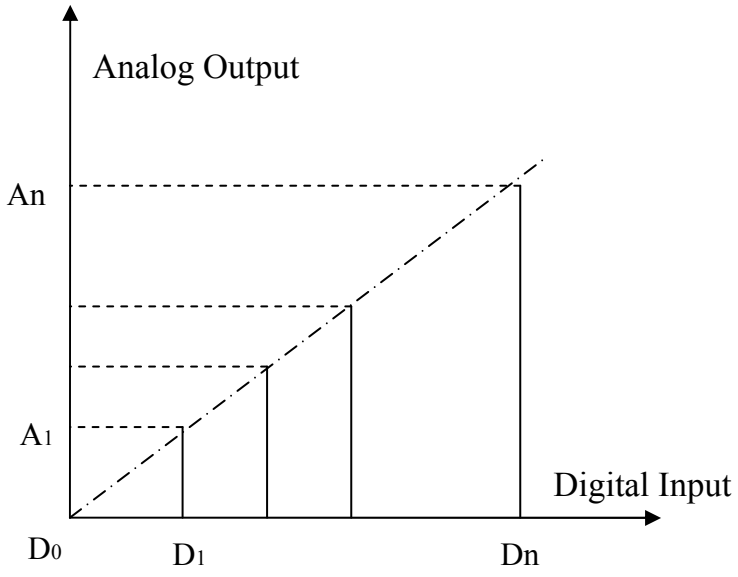

Fig. 2.3: Ideal characteristic of DAC

- Integral nonlinearity (INL) is the maximum deviation of the input/output characteristic from a straight line passing through its end points. The difference between the ideal and actual characteristic is called the INL profile.

- Offset is the vertical intercept of the straight line passing through the end points.

- Gain error is the deviation of the slope of the line passing through the end points from its ideal value (usually unity).

- Settling time is the time acquired for the output to experience full-scale transition and settle within a specified error band around its final value.

- Glitch impulse area is the maximum area under any extraneous glitch that appears at the output after the input code changes. This parameter is also called glitch energy in the literature even though it does not have an energy dimension.

- Latency is the total delay from the time the digital input changes to the time the analog output has settled within a specified error band around its final value. Latency may include multiples of the clock periods if the digital logic in the DAC is pipelined.

- Signal-to-Noise-and-Distortion Ratio (SNDR) is the ratio of the signal

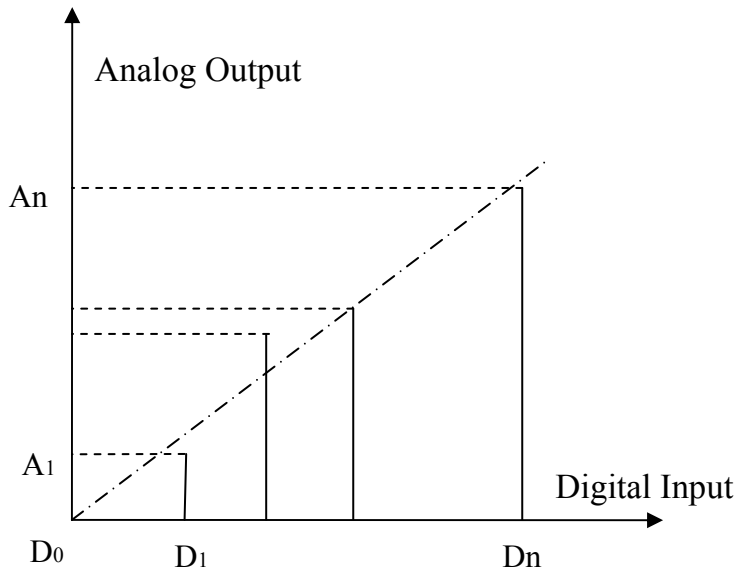

Fig. 2.4: The characteristic of a non-ideal DAC

power to the total noise and harmonic distortion at the output when the input is a digital sinusoid.

Among these parameters, DNL and INL are usually determined by the accuracy of reference multiplication or division, settling time and delay are functions of the loading and switching speed of the output, and the glitch impulse depends on the architecture and design of DAC.

2.3 Mixed-signal testing and mixed-signal BIST

A common architecture for a mixed-signal circuit is shown in Fig. 2.5. It includes analog input components, which are connected to the digital core (e.g. RAM, ROM or DSP) through an ADC. The digital output of the digital core is fed into a DAC, whose analog output is further transmitted to an analog output unit. By the transitional testing method, a Automatic Testing Equipment (ATE) is applied and should provide both analog stimuli for the testing of analog parts (I/O blocks and ADC) and digital testing signals for the testing of digital components (DSP and DAC). Meanwhile, the ATE should be able to deal with the analog response as well as the digital response of the CUT. Such test environment is shown in Fig. 2.6. The ATE is controlled through the tester program, and the tester hardware produces the testing signals (analog and digital)

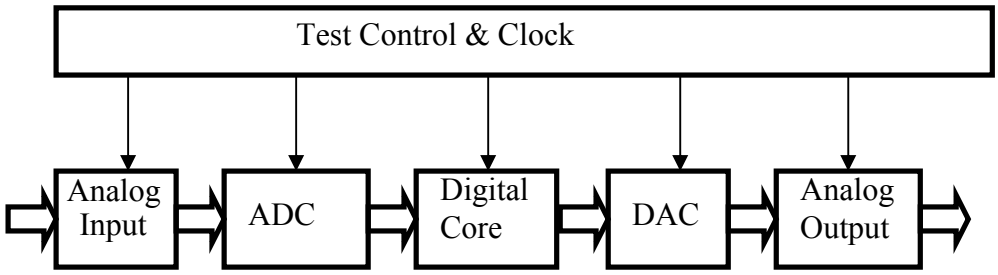

Fig. 2.5: Block diagram of mixed-signal testing

and feeds them into the CUT through a load board, which works as the interface between the ATE and the CUT. The digital response will be feed back directly into the load board and then returns to the ATE for further analyzing. The analog response is fed into the RMS meter on the ATE via a band-pass filter to get the testing parameters of the analog parts. The Phase Lock Loop (PLL) on the ATE provides the primary

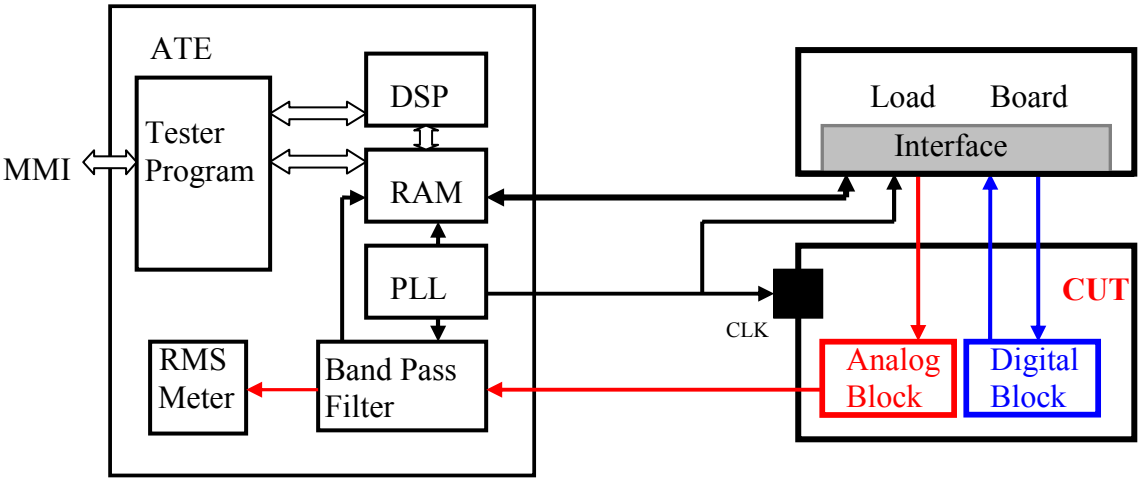

Fig. 2.6: ATE test environment

clock for the ATE, the load board and the CUT as well. The tester program can be modified through the Man-Machine-Interface (MMI) that is typically a workstation based on a UNIX or WINDOWS operating system so that the ATE can carry out different testing tasks as well as test different CUTs. Obviously, this testing environment can easily cause the problems described in Chapter 1.1.

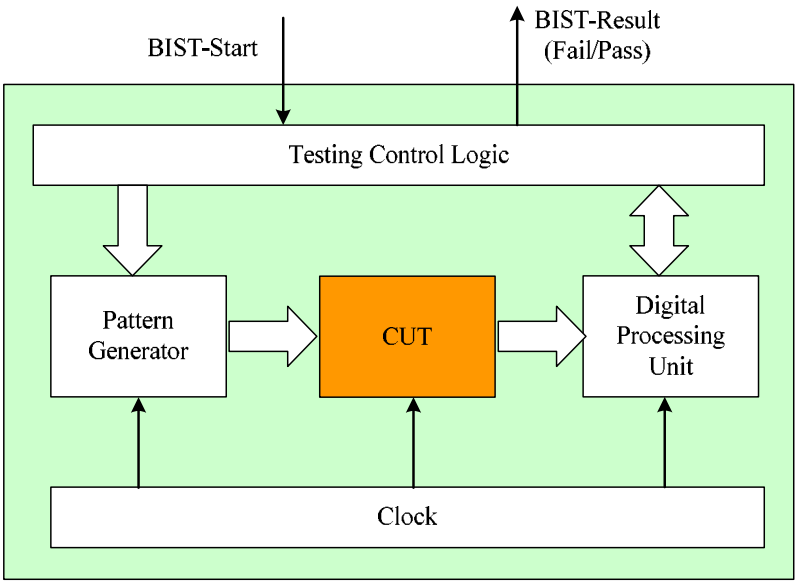

Fig. 2.7: BIST architecture

As an efficient alternative, Built-In Self-Test (BIST) provides a convenient way to carry out the IC testing, whose architecture requires three additional components on chip, namely pattern generator, response processing unit, and testing controller (Fig. 2.7). Examples of pattern generators are a ROM with stored pattern or a chain of D-

flip-flops. As a response processing unit, a comparator with a pre-set value or a linear feedback shift register (LFSR) is a typical implementation instance. A control unit is necessary to activate the test, manipulate the process and analyze the response. In general, several sub-tests can be carried out in one testing process. Sometimes the sampling rate of the CUT is different to that in other blocks (Some examples will be given in Chapter 7). Hence the clock tree stimulated by a primary clock provides the clocks with different rates to the different blocks. It should be pointed out that BIST has some drawbacks yet: it needs overhead, power and additional circuits. Of course, it also needs some layout efforts. However, BIST does provide many advantages in reducing the testing cost. It can overcome many of the signal quality problems associated with the parasitic effects introduced by cables connecting the equipment to the device. Generally, deriving from its nature of on-chip performed test tasks, BIST has the following advantages:

- Costly external test equipment can be avoided.
- Parasitic effects introduced by cables connecting the equipment to the device can be avoided.
- Testing technology can be kept up-to-date with newer-generation integrated circuits.
- Reduction of test time through parallelization.
- Analog multiplexers to make the internal nodes accessible need not to be included in the design.
- Mere manufacturing tests can be extended towards on-field diagnoses: a self-testable device can be examined any time from a remote location.

So it makes sense to refer to the BIST techniques when the additional cost maintains lower than the cost attributed to tester-based methods.

2.4 Present DFT/BIST methods

Recently, many DFT/BIST methods have been reported; some of them are suitable for the testing of only ADC or DAC, while others can be used for the testing of ADC/DAC pairs. A brief overview of these techniques will be given as follows.

2.4.1 Standard BIST structure

In the BIST methods for digital circuits, a widely implemented BIST structure involves a boundary scan technique employing the shift register latches as defined in IEEE Std. 1149.1 [49][50]. This standard provides a set of rules of digital design to facilitate testing at the IC, board and system levels. In order to apply this standard to the mixed-signal field, some more lines are added to IEEE Std. 1149.1, which consumes another two or more pins but remain the compatibility with previously constructed devices. This new method can be looked as a super set of IEEE Std. 1149.1 and is described in IEEE Std. 1149.4. By implementation, two analog pins ATDI (Analog Test Data Input) and ATDO (Analog Test Data Output) are required in addition to the original four digital pins TDI, TDO, TMS and TCK. It allows for the testing of interconnect failure such as shorts and opens, the testing of discrete analog components and networks between ICs and the testing of analog functions within the ICs themselves. A test point can be accessed by connecting either to ATDI or ATDO line with a corresponding analog switch inside the Analog Boundary Scan Cell (ABSC) [51]. An ex-

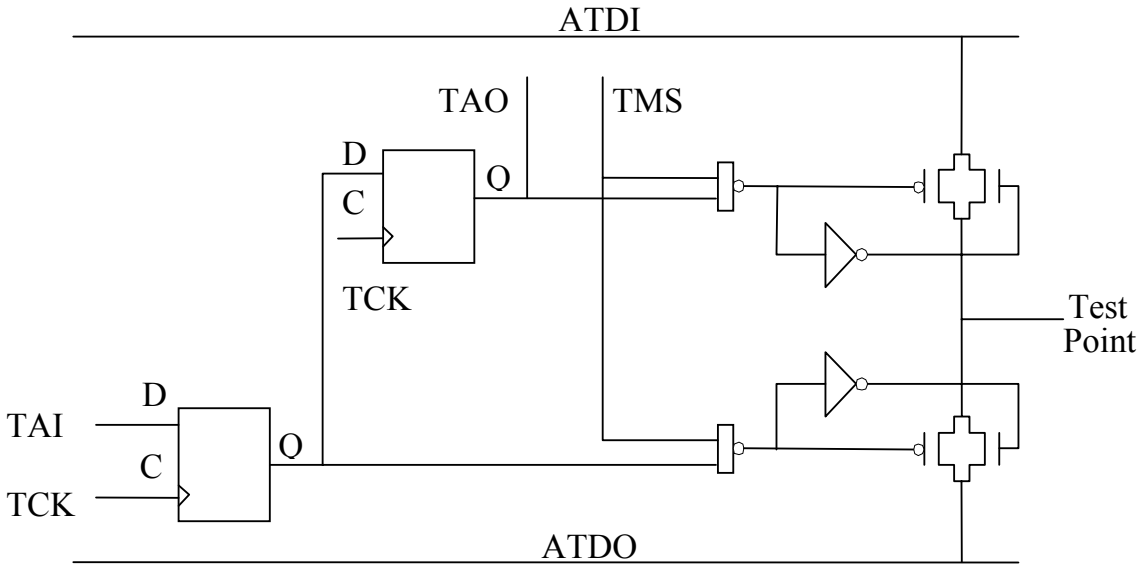

Fig. 2.8: Analog Boundary Scan Cell (ABSC)

ample of the realization proposed in [52] is given in Fig. 2.8. The cell is activated in the test mode by the test model select, where ATDI carries analog test data input signal and ATDO carries analog test data output signals. By using ABSCs, the testing circuits can be decomposed into subsystems and the selected points can be accessed.

The IEEE Std. 1149.4 improves the testability as well as the controllability and observability of mixed-signal circuits. One possible internal structure which supports the

test of interconnection is presented in [53]. It employs the switches together with control logic to form analog boundary scan cells. The switches allow the I/O pins to be connected to functional circuitry for normal operation and to be connected to the ATE for testing operation. The method with reference to IEEE Std. 1149.4 is very effective for complex mixed-signal ICs, but impractical for ICs with only few analog components or low pin count [54].

2.4.2 Multiplexing-based BIST

A Multiplexing-based BIST approach has been presented in [55]. It enhances the observability and controllability of mixed-signal ICs, through isolating the embedded analog components from the digital components by adding the external switching circuitry. The structure is shown in Fig. 2.9. It establishes a digital test mode to test digital parts as well as an analog test-mode to verify analog parts. By implementation, the analog circuitry is isolated from the digital circuitry by adding analog multiplexers before and after each analog macro so that the uncontrolled analog signal will not be able to affect the digital test mode and vice-versa. The shortcomings of this BIST technique are the requirement of extensive clocking circuitry as well as the switching units, which are used for the isolation of analog circuits from digital circuits.

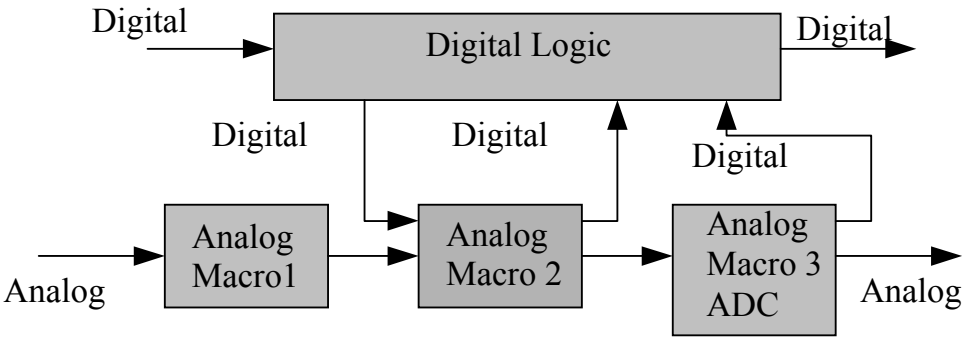

Fig. 2.9: Multiplexing-based BIST

2.4.3 ASIC BIST

A BIST approach for testable mixed-signal ICs has been proposed in [56], which is shown in Fig. 2.10. This approach uses two pins for analog/digital test out, two pins for analog/digital test in, two pins for the scan-in and scan-out paths and several pins

for the control of DFT hardware. The basic idea of this approach is like the method described in Chapter 2.4.2. However, it takes advantage of both the analog multiplexers and digital multiplexers to control and observe the testing signal. Therefore, the observability and controllability for mixed-signal ASIC circuits are greatly enhanced. But, still similar to the method in Chapter 2.4.2, this ASIC BIST is also based on the implementation of clocking and signal circuitry, by which the applicability of this technique is limited.

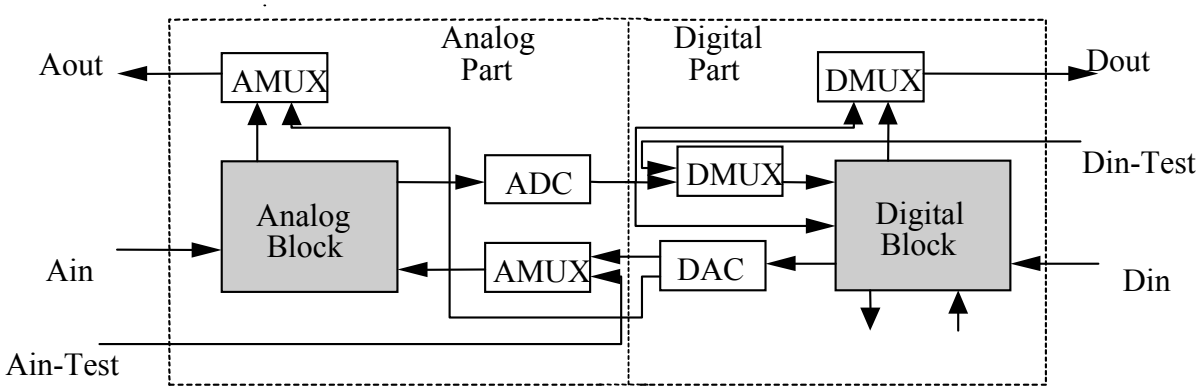

Fig. 2.10: BIST for mixed-signal ASIC circuits

2.4.4 Analog BIST (ABIST)

An analog BIST structure is presented in [58] [59]. A digital scan technique for the digital DFT/BIST testing has been introduced in Chapter 2.4.1. In a similar manner to this digital scan-based testing method, ABIST employs an analog scan to enhance the observability of internal nodes of the analog circuits. The structure of this method is shown in Fig. 2.11. The analog signals are selectively sampled and sequentially transferred through a chain of sampling and hold circuitry. The sample and hold circuits are connected to an analog shift register. For each signal node, input analog multiplexers are used to select and transfer the signal on the tested node. And the analog shift chain is employed to shift out the sampled signal to the output. This analog scan-based DFT method can be used in all kinds of analog circuits.

In fact, conceptually to say, ABIST is not a BIST method but a DFT method, because the main considerations for a BIST method are: I/O isolation, on-chip test stimuli generation, on-chip test response evaluation, on-chip test control, and functional self test for the added on-chip components. Therefore, ABIST is in principle a basic DFT approach.

The main shortcomings of this method lie in the high circuitry overhead, the requirements for clocking circuitry, and the low processing speed for transferring a sampled signal to the output node.

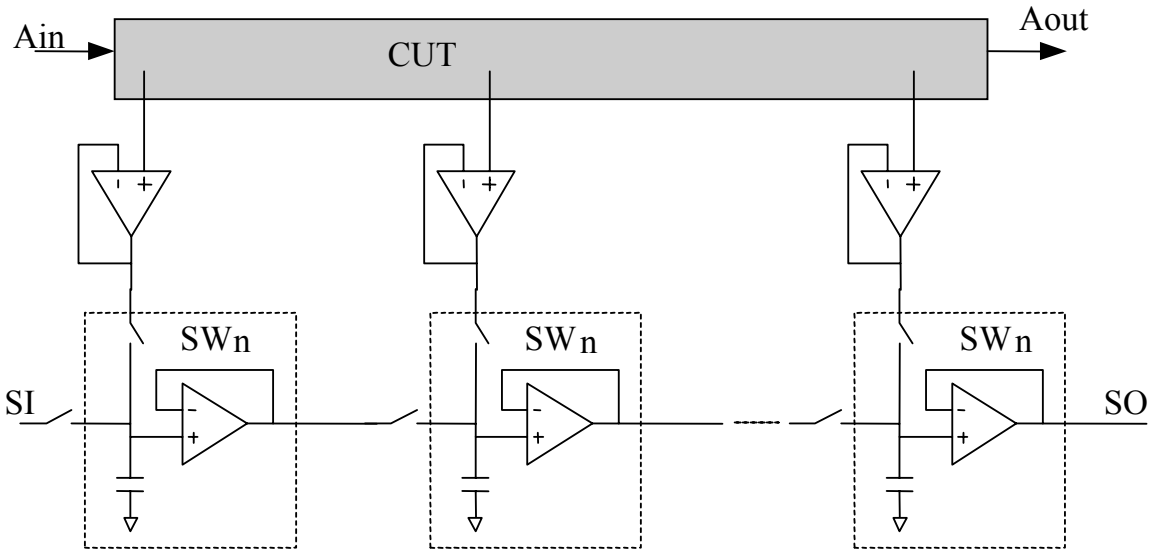

Fig. 2.11: Analog BIST structure

2.4.5 Translation BIST (TBIST)

A BIST structure for testing analog circuits is presented in [60], whose goal is to test if the tested parameters are within the acceptance range. An analog circuit is characterized by a set of special parameters, such as gain, cut-off frequency, delay time, Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), slew rate and others. The principle of Translation BIST (T-BIST) method is based on the conversation of each tested parameter to a DC voltage value, which is proportional to the measured parameter and compared to two predefined values, defining the acceptance range. The key of this technique is the implementation of the detection and translation circuits included in the circuit under test, which detects and translates the measured parameters to the DC voltage. The testing results are stored in a shift register and scanned out in order to decide which parameters failed the test and which passed. The structure of TBIST is shown in Fig. 2.12. A large set of analog multiplexers is used in this structure to choose each circuit under test (CUT) and to route the testing stimuli and the testing response. The integrator translates the test parameter to a DC voltage, and the windows comparator compares the obtained DC value with the two predefined

reference values to verify whether the measured parameters lie in the acceptance range. A shift register stores and scans out the digital response. The main benefits of this method are the high efficiency for functional testing, the high fault coverage, and the detection of very small parameter deviations. But the usage of a large set of analog switches limits its applicability, because the analog switches degrade the analog signal and result in noise and large area overhead.

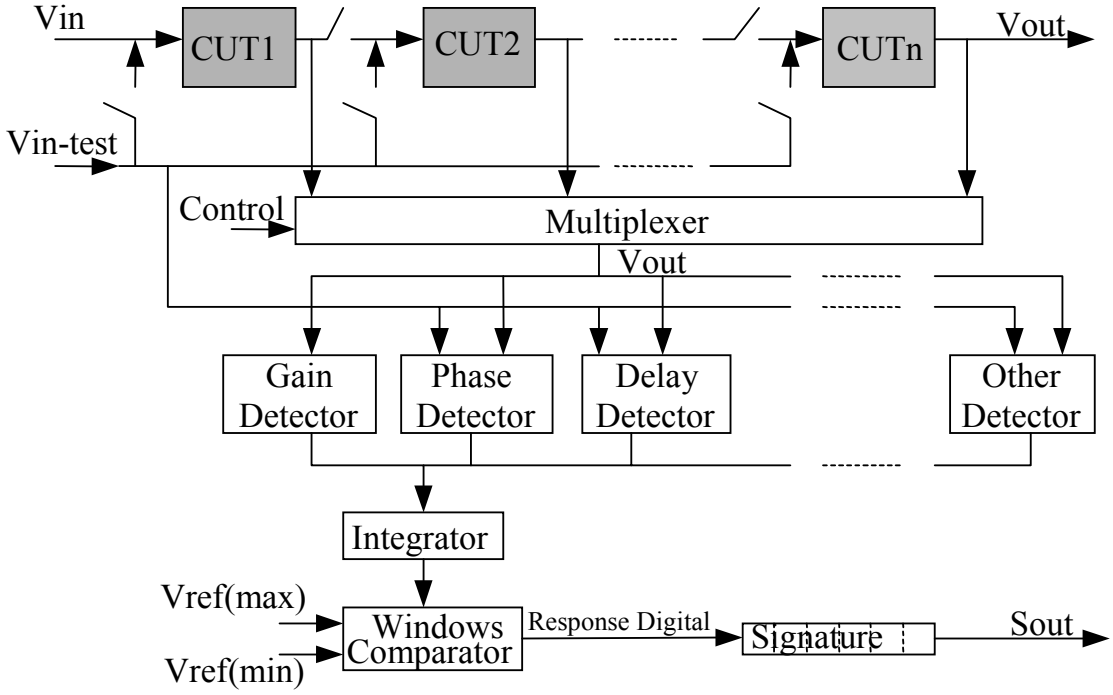

Fig. 2.12: Translation BIST Structure

2.4.6 RBIST

In [37] and [38], a BIST method for testing DAC/ADC pairs is proposed, which is shown in Fig. 2.13. Specifically, tests are designed to measure the Signal-to-Noise ratio, gain tracking, and the frequency response of a sigma-delta ADC. The stimulus generator is a precise multi-tone oscillator designed for an uncalibrated environment. The digital sinusoidal waveform output of the resonator is modulated through a Delta-Sigma Modulator (DSM) into a Pulse Density Modulation (PDM) bit stream so that all the noises are pushed to the higher frequency. This PDM stream can be produced off-chip and stored in ROM/RAM on-chip, and then it will be fed through an on-chip analog Low Pass Filter (LPF) to filter out the noise in the higher frequency. Thus an accurate analog sinusoidal stimulus can be obtained [39] [40]. The design of the oscillator

is fully digital, except for an imprecise low-pass filter, and it is digitally programmable for multiple amplitudes, frequencies, and phases.

By testing steps, firstly, the digital sinusoidal signal produced digitally in an on-chip micro-processor will be fed into the signal generator, which consists of a Delta-Sigma Modulator (DSM), a 1-bit DAC and an analog LPF, to produce an analog voltage. This analog sinusoidal signal will traverse through the multiplexer into the ADC, and the digital output of the ADC will be analyzed in the DSP unit. Secondly, after the ADC is verified, the DAC will be verified. The digital sinusoidal signal will be transmitted directly into the DAC and through the switch, the multiplexer, the verified ADC and into the DSP unit for the post-processing. At last, if both the ADC and the DAC are verified and there is any other analog component under test, we can take advantage of the ADC, the DAC and the on-chip signal generator to form an analog tester to verify other analog circuits. This method can bring many benefits such as testing the ADC/DAC pairs simultaneously and reducing the hardware overhead. But the application of this approach is limited to such cases that the resolution of the ADC must be at least 2-3 bits higher than that of the DAC. Otherwise, the DAC would degrade the whole performance of testing path and, consequently, the ADC can not be measured correctly.

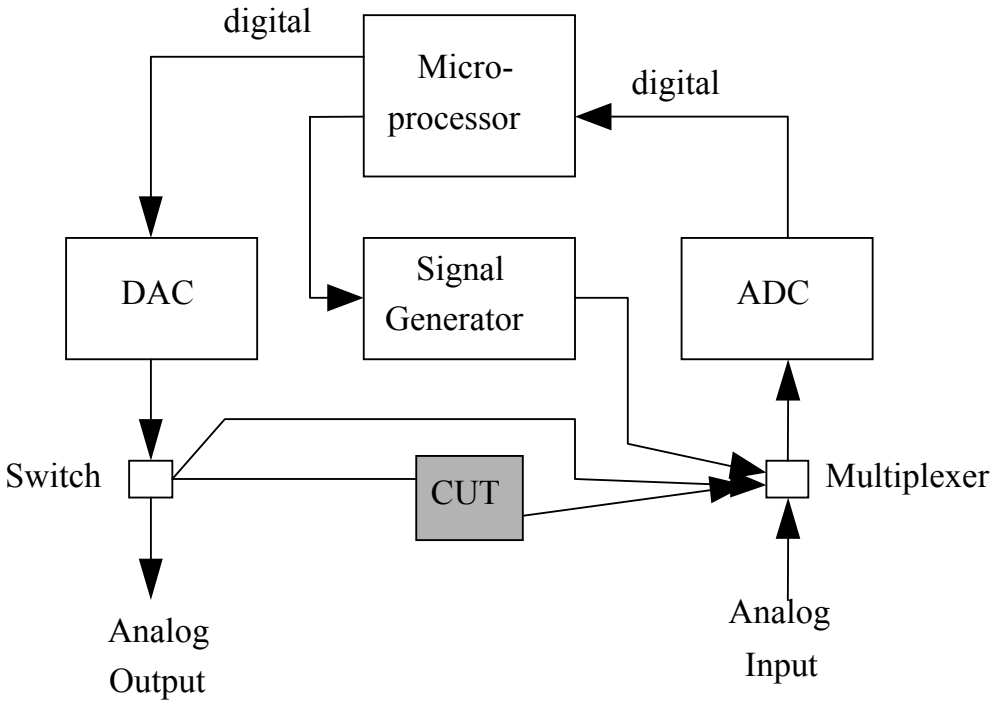

Fig. 2.13: The structure of mixed-signal BIST

2.4.7 Oscillation BIST

In [41] and [42], the authors present a low-cost test method called oscillation-test for analog integrated circuits. The basic idea of this method is illustrated in Fig. 2.14. It is very difficult to measure the analog CUT output directly owing to its analog nature. But the testing of frequency is relatively easy by using a counter to count the incoming point's number in a pre-defined period. In the oscillation BIST mode, the Circuit under Test (CUT) is converted to a circuit which oscillates through rearranging the CUT. Faults in the CUT which cause a reasonable deviation of the oscillation frequency from its nominal can be detected. Assuming that $H(j\omega)$ is transfer function of the CUT, the designer can implement an additional circuit $N(j\omega)$ on chip so that $H(j\omega)\cdot N(j\omega)=-1$ (the oscillation condition) is achieved and that the whole system $F(j\omega)$ would oscillate at a certain frequency, which would reflect the character of $F(j\omega)$. Thus, a simple counter can be used, which counts the frequency of $F(j\omega)$ to get the feature of $H(j\omega)$. In fact, this BIST approach is an analog-to-frequency (or analog-to-time) converter and it is more like a structure oriented testing than a function oriented testing. By using this method, the test vector generation problem is eliminated and the test time is greatly shortened because only a limited number of oscillation frequencies are evaluated for each CUT. Nevertheless, the impact of control logic delay and the imperfect analog BIST circuitry on the test accuracy are not clear. And this method depends on the presence of a DSP. Moreover, the BIST designers should have both a good understanding about the structure of the CUT and some good knowledge of the analog/mixed-signal circuits design. At last, the oscillation BIST approach is very hard for the application of the Computer Aided Design (CAD) technique, which limits its commercial perspective.

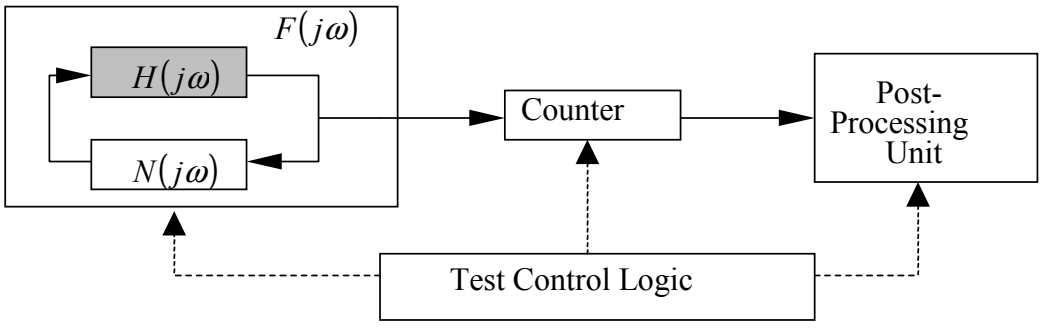

Fig. 2.14: Oscillation BIST

2.4.8 Histogram BIST

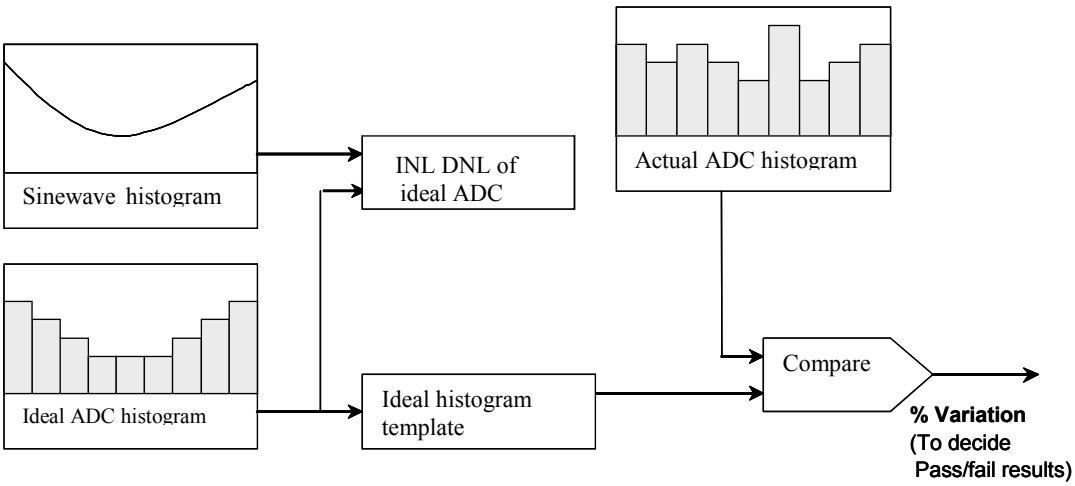

Fig. 2.15: Histogram for ADC BIST

In [43] and other related articles, a sinusoidal histogram BIST implementation for the ADC testing is proposed, which is illustrated in Fig. 2.15. Given an analog input signal, the histogram shows how many times each different digital code word appears on the ADC outputs. The ADC errors modify the count of the output codes and so impact the histogram shape. As a result, comparing the measured histogram to the ideal one and computing some calculation leads to evaluate some ADC parameters such as offset, gain, DNL and INL.

Fig. 2.16 shows a top level structure of a Histogram BIST for an analog component. The goal of this proposal is to test static parameters. The benefit is that this approach can cover most error-sources. But this method suffers from several limitations: firstly, the number of input patterns is so huge that the testing time is much longer than that of other methods (e.g. Oscillation BIST, or HBIST to be introduced later), secondly, the

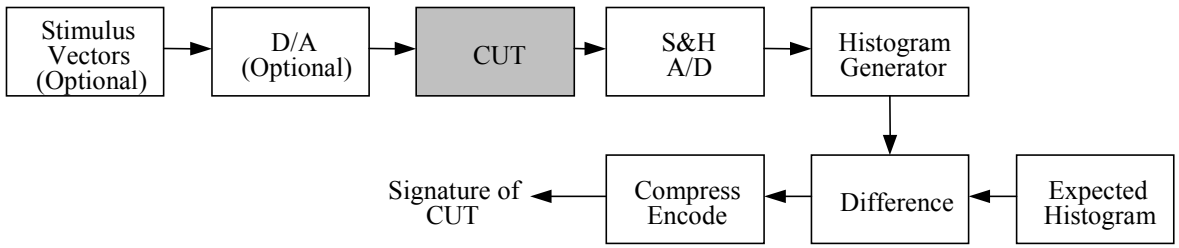

Fig. 2.16: Histogram BIST

CUT should work in a predefined range. Otherwise, the range of patterns would be too big to be realized on chip economically. The presence of RAM and DSP on chip is also a limiting requirement for the application of this method.

2.4.9 Polynomial BIST

An alternative method – polynomial BIST – is presented in [44], which refers to approximating the transcharacteristic of an ADC with the best fitting a 3rd order polynomial. The coefficients of this 3rd order polynomial will be derived from the digital output of the CUT (ADC), which is based on accumulators working on chip. After a sinusoidal stimulus is applied to the CUT, the offset, gain, and harmonic distortion that would be imparted to this input will be computed out. The benefit of Polynomial BIST is that this method is very simple and fast. But the limits lie in that it is very sensitive to the noise level and it needs DSP-core on chip. Similar to the Histogram BIST in Chapter 2.4.8, the polynomial BIST needs a relative accurate analog sinusoidal stimulus on chip as well. But the generation of an analog sinus signal on chip is not an easy task for the designers. Fortunately, not all the BIST methods need such stimulus. E.g., HBIST and Fluence BIST to be presented in the following have no such restriction.

2.4.10 HBIST

The HBIST is proposed in [45]. By this BIST approach illustrated in Fig. 2.17, a Pseudo-Random Bit Sequence (PRBS) generated by a Linear-Feedback Shift Register (LFSR) is fed into the digital side of the DAC as testing stimulus. A Multi-Input Shift Register (MISR) will compact the digital output of the ADC to generate a signature

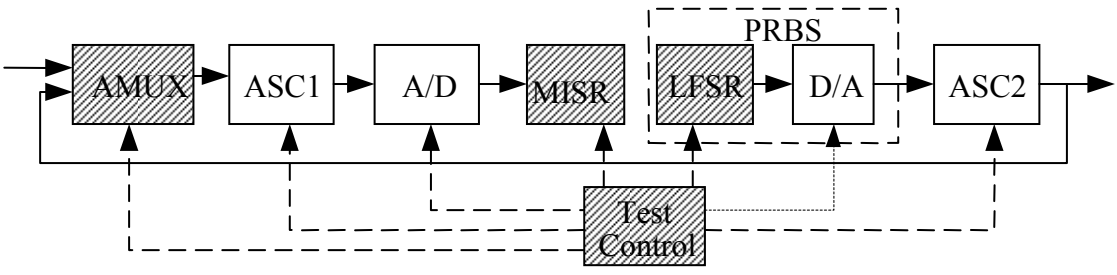

Fig. 2.17: The Structure of HBIST

which is compared to a value stored in memory. The goal of this method is the static/dynamic parameters testing of the ADC/DAC pairs. Its advantage is that its hard fault coverage is very high (above 95.5%). However, the restrictions are that it needs a powerful digital core on chip; both ADCs and DACs must be on chip; and the faults of the ADCs (or the DACs) might be masked by the DACs (or the ADCs) during the test. Moreover, there should be enough area for the design of LFSR, because the store of the sinusoid waveform needs lots of registers. Besides this, the presence of a DSP is also an important condition for applying the HBIST method.

2.4.11 Fluence BIST

A new approach has been presented for the DAC-BIST shown in Fig. 2.18 [46]. This method employs a Delta-Sigma (∑Δ) modulator to form an oscillation loop. Then the tested parameters can be extracted from the output of this ∑Δ structure. This procedure takes advantage of the principle of the oscillation BIST technique. By testing the DAC parameters (offset, INL. DNL), the DAC input is switched between two different and opposite signs codes HI Input and LO Input. An up/down counter evaluates the average of the PDM stream over a period time. Then the result will be compared with the theoretically evaluated value; at last, the code (HI Input – LO Input) associated distortion is derived.

The benefit of this method is that it can test a DAC individually without the help of an ADC on chip. And due to the usage of a ∑Δ modulator, the need of high precision test hardware is eliminated. Moreover, there is no need for producing the test stimuli. This

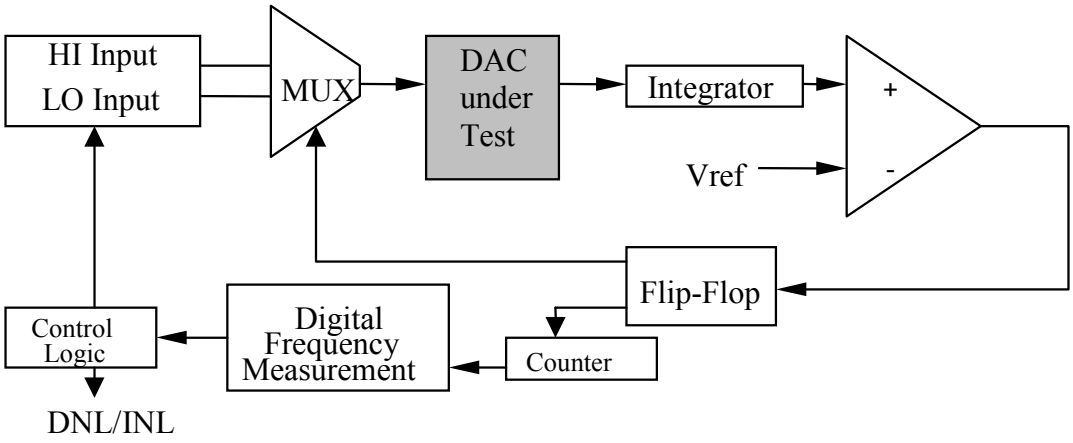

Fig. 2.18: INL/DNL testing for DAC BIST

method extracts both the static parameters (INL, DNL and offset) and the dynamic parameters (clock feed through) of the DAC under test. But the usage of a ∑Δ modulator needs large area on chip, which limits the application of this approach; moreover, the possible need of a DSP for the dynamic parameters testing is also a problem for the BIST design. This approach can be employed for the testing of an individual DAC without an ADC on chip. In addition, the sampling rate of the ∑Δ modulator must be the same as the clock of the CUT (DAC). So the design of the ∑Δ modulator, esp. the design of the operation amplifier (OPA) in the integrator of this modulator, is very important. This method is only suitable for the testing of the relative low speed DAC, since the design for the ∑Δ-Modulator with a high sampling frequency would be a big challenge.

Although some BIST methods published in [47] [48] are excluded in this dissertation, the most important BIST achievements have been summarized in this work. Such summary is concluded in Table 2.1. Since each application has specific needs as well as some limits by implementation, there are no common rules by designing a mixed-signal BIST method, which means there is no a universal BIST approach for mixed-signal circuits testing. An understanding of how to apply a BIST method to particular analog and mixed-signal circuits requires a good understanding of the BIST guidelines and concepts. However, the following key-points should be kept in mind by a BIST concept and design engineer:

- BIST method is only one of the alternative methods for reducing the testing cost, but not *always* the best one.

- The resolution of the BIST circuitry must be at least 2-3 bits higher than that of the Circuit under Test (CUT).

- The BIST should not cause instability of the CUT nor degrade the performance of the CUT; in other words, the CUT should work in the acceptance range by no-test mode.

- The additional cost (due to the additional chip overhead, additional design efforts and others) should be covered by the saved cost (due to the reduction of total testing time or the usage of cheaper testing equipment).

- On the one hand, the BIST solution should reuse the on-chip resources as much as possible to reduce the area overhead; on the other hand, the proposed solu-

tion should be a structural one (black boxes), which enhances the maintenance-ability.

- The BIST circuitry should have the character of functional singleness. The BIST circuitry is only designed for testing of the CUT and should be active only in testing mode. In functional mode, it should be isolated from the CUT, so that it has not any effect on the CUT at all and seems to disappear completely from the chip.

- The self-test and self-verification function of the BIST circuitry is non-dispensable and should be carried out before the other testing steps. The BIST design should consist of three steps: 1) the self-test of BIST circuitry; 2) the BIST testing process; 3) the isolation of BIST circuitry from the CUT.

Although it is stated that there is no a universal BIST approach for testing the mixed-signal circuits, this work intends to figure out some useful rules by designing a BIST approach for the dynamic testing of the ADC/DAC pairs, because the DAC and the ADC are the two most widely used mixed-signal components and often used in pairs in practice. According to the reports from the industry [4] [62] [77], the SNR testing of the ADC/DAC pairs is very time-consuming and is one of the important factors contributing to the high testing cost. Therefore, in the following chapters, the design of a BIST approach for testing the ADC/DAC pairs will be discussed.

Table 2.1: The different BIST approaches (Part 1)

BIST Type	Testing Goal	Resolution	Components	Resource		
				Overhead	Time	Power
RBIST	ADC/DAC (SNR)	High	Switch, MUX & ana. LPF	Middle	Middle	Low
Oscillation BIST	Structure DFT	Depending on parameter ranges	Rearranging CUT for Oscillation	Little	Fast	Low
Polynomial BIST	ADC(INL, DNL&SNR)	Low	MUX,Control Logic,RAM&DSP	Large	Middle	High
Histogram BIST	ADC (INL&DNL)	High	DSP,RAM and ROM	Large	Slow	High
HBIST	ADC(INL, DNL&SNR)	High	DSP,ROM and LFSR	Middle	Middle	Middle
Fluence BIST	DAC(INL,DNL)	High	Delta-Sigma Structure and Reg.	Middle	Slow	Middle

Table 2.1: The different BIST approaches (Part 2)

BIST Type	Stimuli	Response Measurement	Requirement	Remark
RBIST	Sinusoidal signal	1)FFT;2)IEEE 1057;3)Notch Filter	ADC better than DAC; DSP	Test Example: 16-Bits ADC
Oscillation BIST	No Need	Frequency Extraction by Counter& Parameter Extraction by DSP	Good Analog Knowledge for Designer	Not suitable for some cases
Polynomial BIST	Ramp & Sinusoidal signal	Polynomial Fitting & DSP	On-chip DSP & low noise level	Fitting only to 3rd harmonic distortion
Histogram BIST	Sinusoidal signal	Hist-generation& Comparison	A standard Histogram before BIST	Test Example: 12-Bits ADC
HBIST	Pseudo-Random Bit Sequence	Signature Generation by LFSR & Comparison	A standard Signature before BIST	Hard-fault coverage up 95%
Fluence BIST	No Need	Counter	Opposite Codes in Registers	Test Example: 8-Bits DAC

Chapter 3

The BIST Concept for ADC/DAC Pairs

Mixed-signal devices bridge the gap between the analog and digital devices or functional blocks. Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) are the two most common and important mixed-signal components in this class. ADC provides the interface from the analog part to the digital domain; meanwhile DAC sets up the bridge from the binary digital domain to the analog world. The converters are widely used in the most modern measurement, control instrumentation and systems. They are also employed in pairs by the applications in the fields such as wireless telecommunications, data exchange systems and satellite communications systems. And the testing of ADCs and DACs is a very hard task for the test engineers because of the analog nature of these two devices. Besides the expensive mixed-signal testing devices, the long testing time of ADC/DAC is also a significant factor contributing to the high testing cost. Thus, many efforts have been made and are being made to reduce the ADC/DAC testing costs [37]-[48], which have been addressed briefly in Chapter 2.4. But some of these methods deal with the testing of a solo ADC; and some of them are only concerned on the ADC/DAC pairs for the particular case. None has given an overview of the BIST strategy for the ADC/DAC pairs; and none has provided a BIST solution for the DAC SNR testing, either. In this chapter, the BIST test strategy for ADC/DAC pairs based on the loop-test will be introduced. And a BIST approach for the DAC SNR testing embedded with the loop test will be proposed in Chapter 7.

3.1 The circuit under test – the ADC/DAC pairs

The purpose of this work is to figure out some common rules for the BIST design for the testing of the ADC/DAC pairs. A typical application case of the ADC/DAC pair is

shown in Fig. 3.1. Two opposite paths dedicated to different tasks are distinguished: the one on the DAC line outputs the digital incoming to the analog domain; the other one, on the ADC line, sends the sampled analog signal from input to DSP core.

The DAC path contains digital filters, a DAC, analog post filters and amplifiers to adjust the gain of the signal. The incoming signal from the digital domain is at first fed into digital filters, by which the bandwidth of the signal is limited in order that it would not fall outside the frequencies range of the following DAC. Moreover, in most cases, the clocking rate of the incoming binary digital data stream is different from that of the DAC (e.g. by a codec chip, the typical sampling rates of sound, voice mono, voice stereo, music mono, music stereo are: 8, 16, 32, 44.1, 48kHz, while a voice-band DAC operates at a fixed frequency of 4MHz). So the digital filters are served often as interpolation/decimation filters, too. After DAC converts the digital signal into analog signal, the reconstruction analog filter smoothes and outputs the desired analog signal. In some cases of such transmitter system, the analog signal should be adjusted by the gain and sent out for the further processing (e.g. to antenna).

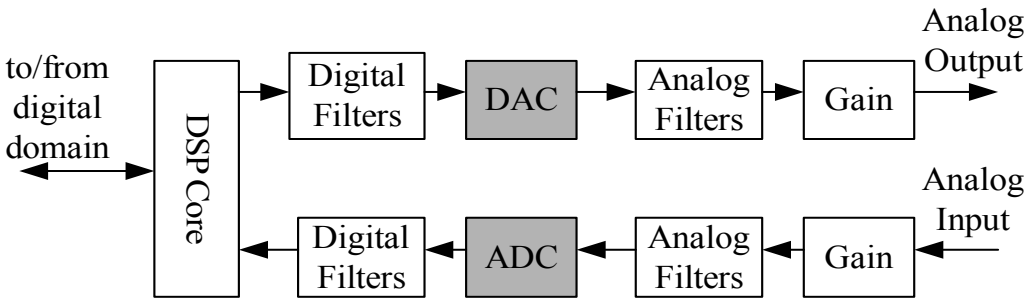

Fig. 3.1: Block scheme of the ADC/DAC pairs

The ADC path consists of an amplifier, an analog anti-aliasing filter, an ADC and digital post filters. The purpose of the anti-aliasing filter is to avoid the overlapping of the signal when it is re-sampled. The digital post filters are still often used as multi-rating filters so that the ADC can work at a fixed frequency.

3.2 Traditional test concept for the ADC/DAC pairs

Testing of the circuit described above is currently performed via analog and digital multiplexers that make certain internal nodes accessible to the external equipment

when the circuit is in test mode. A digital sinusoid signal is sent just before the DAC and the output collected at the analog output; in this way relevant measurements can be made on the analog side of D/A path. Similarly, an analog sinusoidal waveform is sent through at analog input and collected just after the ADC to evaluate the ADC path's performance. The testing machines contain high-quality digitizers which sample the analog responses of the CUT to the stimuli. Signal power estimations are made via the Fast Fourier Transform (FFT).

In particular, in production tests the following quantities have to be determined:

- Signal-to-Noise Ratio (SNR)
- Signal-to-Noise-and-Distortion Ratio (SNDR)
- Total Harmonic Distortion (THD)
- Power supply rejection
- Idle channel noise

While the meaning of the first three quantities is clear, an explanation may be necessary for the last two. During *power supply rejection test* a ripple, or a high-frequency sinusoidal waveform is applied to the converter's supply line to check that the device remains stable and reliable; *idle channel noise* is a measurement of the noise at the output in the absence of input.

It is also possible to internally connect certain points, in particular the digital sides of the two converters (or the analog sides as well) so that a test loop is generated that appears all analog. An analog signal is sent from the analog input and the analog output is collected at the output node.

As known, the mixed-signal testing equipments are very expensive. Furthermore, such testing for the DAC and ADC is very time-consuming, because the set-up time of the analog filters is very long and the large set of the switching circuitry in the converters occupy also much testing time. According to some industrial report [62], the testing time for the converters is 73% of the whole testing time for the analog macro, and ¼ of the total testing time for the wafer-test. Then, in the following, a BIST strategy for the ADC/DAC pairs based on the loop test will be discussed. With this method, it is possible to test the ADC/DAC pairs on chip without the aid of the expensive external mi-

xed-signal testing equipments, or to use a simple but relatively much cheaper digital-driven ATE to finish the complex mixed-signal testing tasks. Moreover, the total testing time could decrease through parallel test, which reduces the total test cost further.

3.3 BIST strategy for the ADC/DAC pairs based on loop test

In order to reduce the total testing cost, a new test concept has been developed and is illustrated in Fig. 3.2. The strategy is to short-circuit the ADC and the DAC paths on the analog side in test mode so that the looped circuit appears all digital. The signals necessary for the functional tests of the analog components are generated with the aid of the extra hardware on chip. They are then applied to the digital-to-analog converter and fed into the loop. After sampling with the analog-to-digital converter, the received signals are evaluated again using some digital signal processing methods implemented on chip as well. In this way it is verified if the performance of the analog components falls within the specification limits.

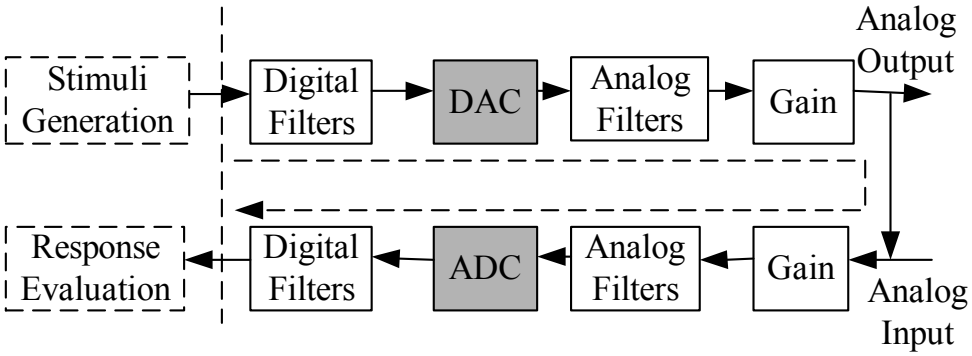

Fig. 3.2: Block scheme of loop BIST

But it should be noted that the test path is one way and there are perhaps different specifications for the DAC and ADC paths. For instance, by a type of codec chip for GSM/CDMA systems, the DAC path, in fact, must meet a performance of SNR = 90dB whereas the ADC path of SNR = 70dB. If the first tract didn't have a higher performance than the second, it would degrade the signal to a point below the second tract's specifications and the loop test would not give any advantage. Therefore, the path with eventual higher performance should be tested first, and then the loop test can be performed to verify another path. Thus, there are mainly three steps in the loop-BIST:

1) Verify the path with higher performance. This can be completed through the usage of external ATE or solo ADC BIST (If ADC path is better than DAC path) or DAC BIST (if DAC path is better than ADC path).

2) Short circuit the analog side of the ADC and DAC paths to form a digital loop.

3) A fully digital driven loop test to verify the rest path. The digital testing stimulus, which can be either generated on chip or produced through the external ATE, is driven into the loop. The test response from the loop is evaluated and compared with the reference value. Similarly, the response evaluation is carried out either on chip or by the external ATE.

It should be noted that ATE cannot be totally forgotten. Depending on the available resources such as on chip overhead, external testing equipment, time to tape-out etc., the ATE can be combined with the BIST approach flexibly to form varied BIST solutions, which are illustrated in Fig. 3.3. The verification of solo DAC and ADC can be executed both through the external ATE and by the implementation of DAC-BIST or ADC-BIST on chip. Similarly, the testing stimulus and the response evaluation can be provided by the ATE or built on chip. An economic combination of ATE and BIST should be chosen according to the concurrent situation. The chips can be tested on the ADC side by a concurrent use of BIST or an ATE. Moreover, the BIST's stimulus generator can be used independently on the response evaluation algorithms, while external equipment picks up the output and measures its power characteristics.

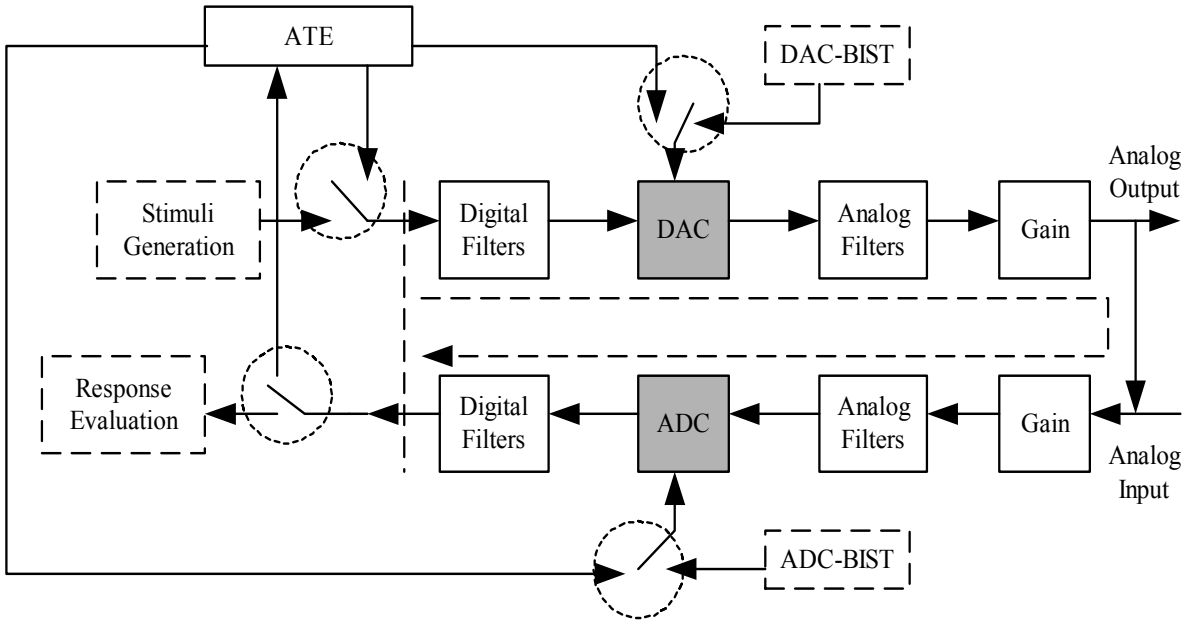

Fig. 3.3: Block scheme of BIST and ATE

In order to make the research more applicable, this dissertation is concerned about a fully on chip BIST solution for the dynamic loop BIST (SNDR testing). Not only have the verifications of solo DAC and ADC been executed by on chip DAC-BIST and on chip ADC-BIST, but also the stimulus generation and response evaluation blocks are implemented on chip. The result is that the approach does not depend on the presence of external ATEs. It has been mentioned that in the loop BIST one branch can happen to be yielded lower than another branch, which means that there are three different cases by the loop BIST: ADC branch has a lower yield; DAC branch has a lower yield; or the two branches have the same good performance. Therefore different solutions for these different situations will be discussed as follows

3.3.1 Case 1:

If the performance of ADC path is better than that of DAC path, the ADC path must be verified first. After that, the DAC path can be measured with the verified ADC path. The Loop-BIST structure is illustrated in Fig. 3.4. Two analog multiplexers are inserted to the analog parts of the converters. Two digital multiplexers are added to the digital parts of the paths and connected with the stimulus generation and response evaluation blocks respectively. One switch and one multiplexer are employed, surrounding the ADC with better performance. The multiplexer is connected with the ADC-BIST functional block and will be switched on in the ADC BIST mode. The switch will isolate the tested ADC from other circuits in the ADC BIST mode. They will be switched on in the loop test mode and normal configuration (non-test mode). Fig. 3.5 shows the testing algorithm in a data-flow form.

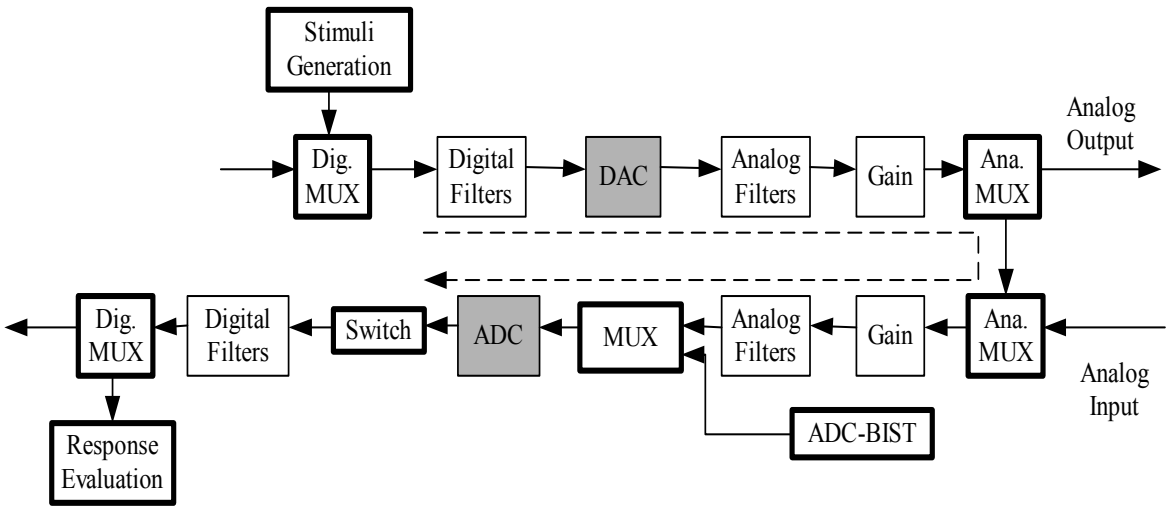

Fig. 3.4: Block scheme of Loop BIST and ADC BIST

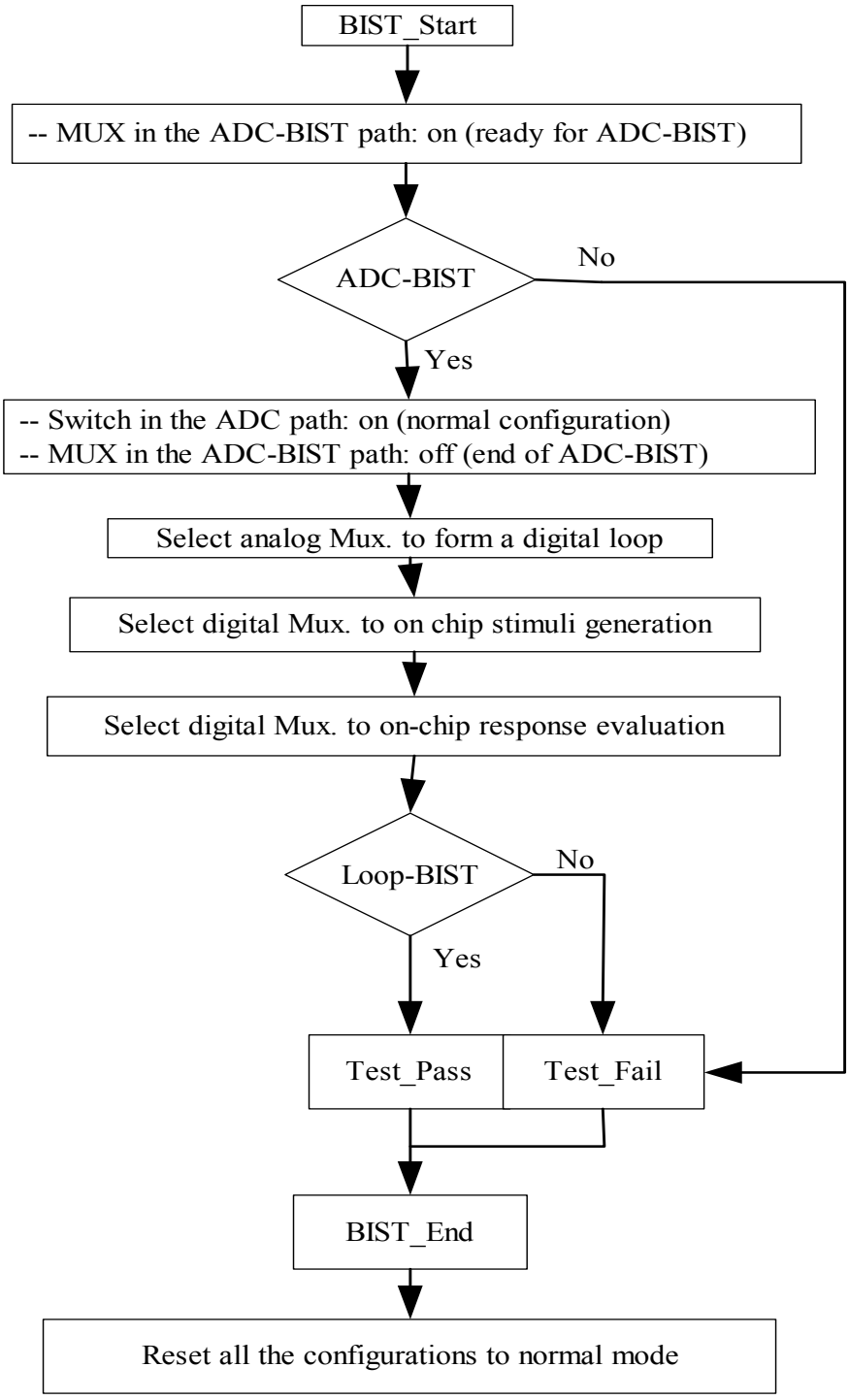

Fig. 3.5: Algorithm of loop BIST and ADC-BIST

3.3.2 Case 2:

If the performance of DAC path is better than that of ADC path, the DAC path must be

verified first. After that, the ADC path can be measured with the verified DAC path. The Loop-BIST structure is illustrated in Fig. 3.6. Two analog multiplexers are inserted to the analog parts of the converters. Two digital multiplexers are added to the digital parts of the paths and connected with the stimuli generation and response evaluation blocks respectively. One multiplexer and one switch are employed, surrounding the DAC with better performance. The multiplexer is connected with the DAC-BIST functional block and will be switched on in the DAC BIST mode. The switch will isolate the tested DAC from other circuits in the DAC BIST mode. They will be switched on in the loop test mode and normal configuration (non-test mode). Fig. 3.7 shows the testing algorithm in a data-flow form

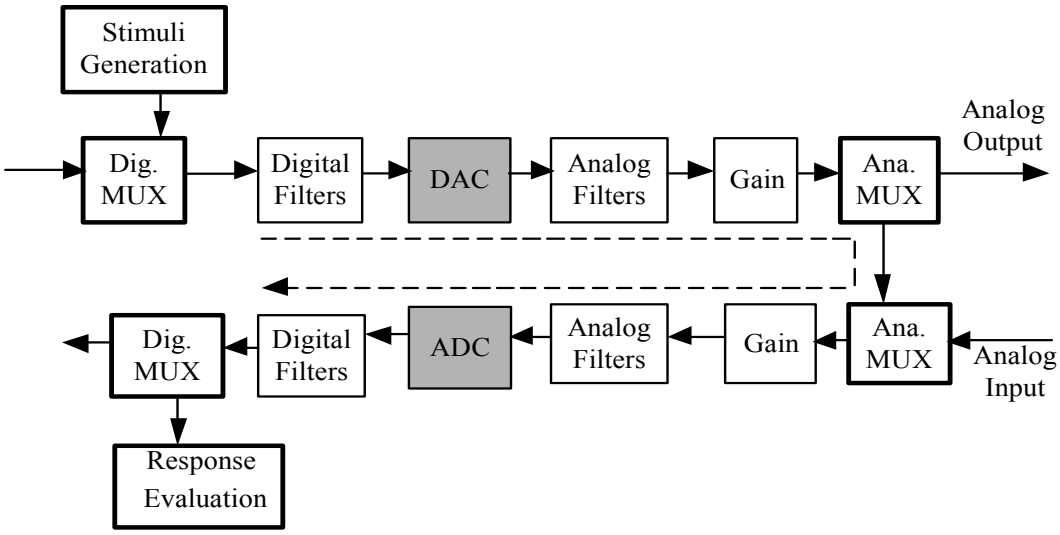

Fig. 3.6: Block scheme of loop BIST and DAC BIST

3.3.3 Case 3:

If the performance of ADC path and that of DAC path are identical, the ADC path and the DAC path can be verified at the same time. The Loop-BIST structure is illustrated in Fig. 3.8. Two analog multiplexers are inserted to the analog parts of the converters. Two digital multiplexers are added to the digital parts of the paths and connected with the stimuli generation and the response evaluation blocks respectively. In test mode they will be so selected that the ADC path and the DAC path are rearranged to form a fully digital loop. Fig. 3.9 shows the testing algorithm in a data-flow form.

Obviously, the on chip signals generation and the on chip response evaluation blocks

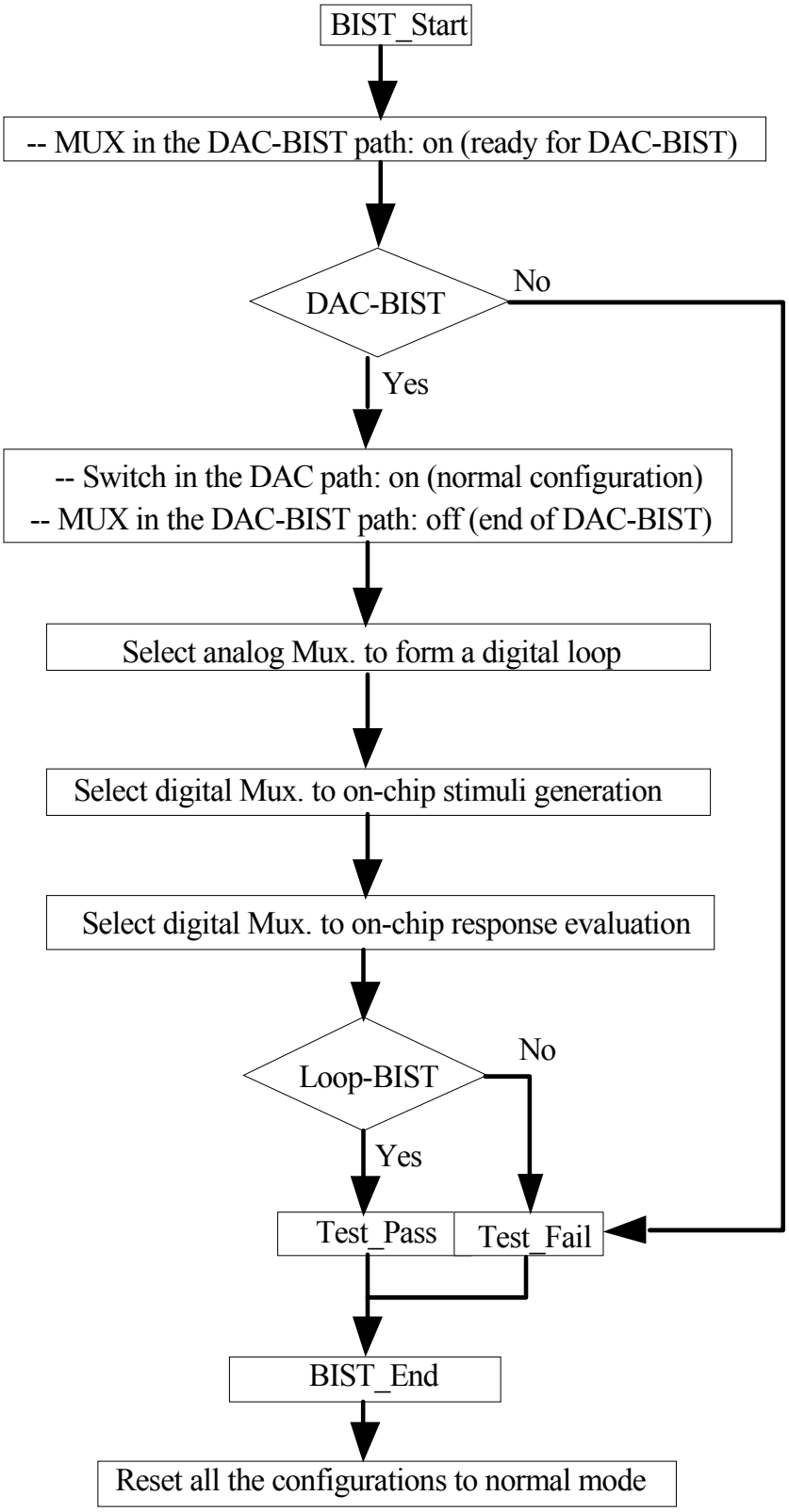

Fig. 3.7: Algorithm for loop BIST and DAC BIST

are two important functional blocks for the loop-BIST. In the following chapters, the signal generation technique and on-chip response evaluation methods will be intro-

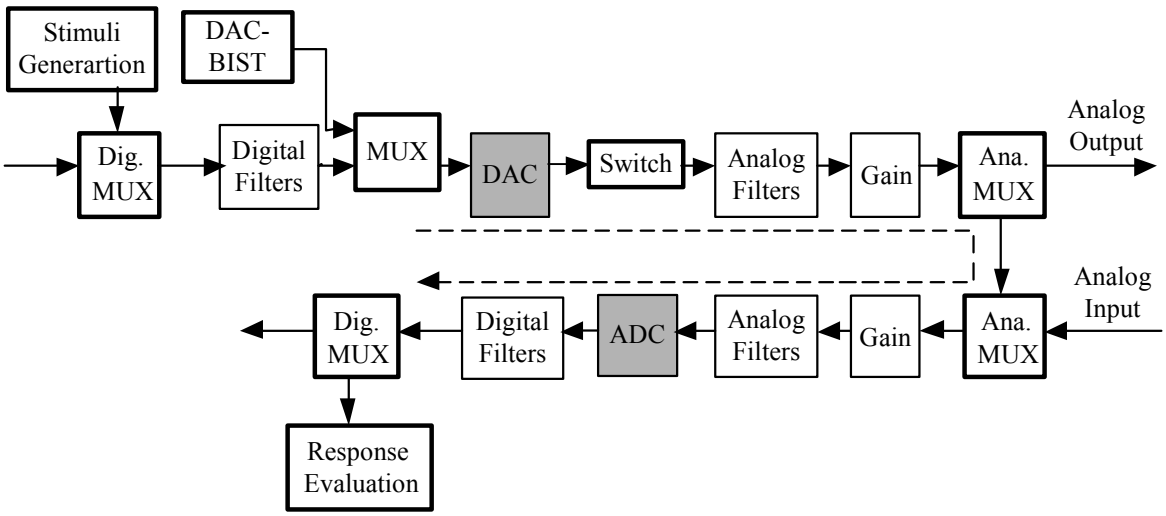

Fig. 3.8: Block scheme of loop BIST

duced. Three concurrent cases will be also studied further and the corresponding loop-BIST implementations are proposed in the following contents, which include the concurrent DAC-BIST technique and ADC-BIST technique, too. It should be noted that a typical class of filter, so-called Wave Digital Filter (WDF), has been widely adopted in this work, because the WDF has the following properties:

- Able to be realized due to the absence of no delay-free loops.
- Low sensitivity of transfer function to coefficient variations.
- Considerable overhead saving through “shift-and-add” multipliers.
- Least number of multipliers and delays which equals to the filter degree.
- In the specific application, WDF allows resource reutilization.

This is also why WDF is important for this work. Therefore, in the next chapter, a brief introduction about some basic principles of Wave Digital Filter (WDF) will be present along with its interesting mathematical approach to filter design and some implementation issues as well.

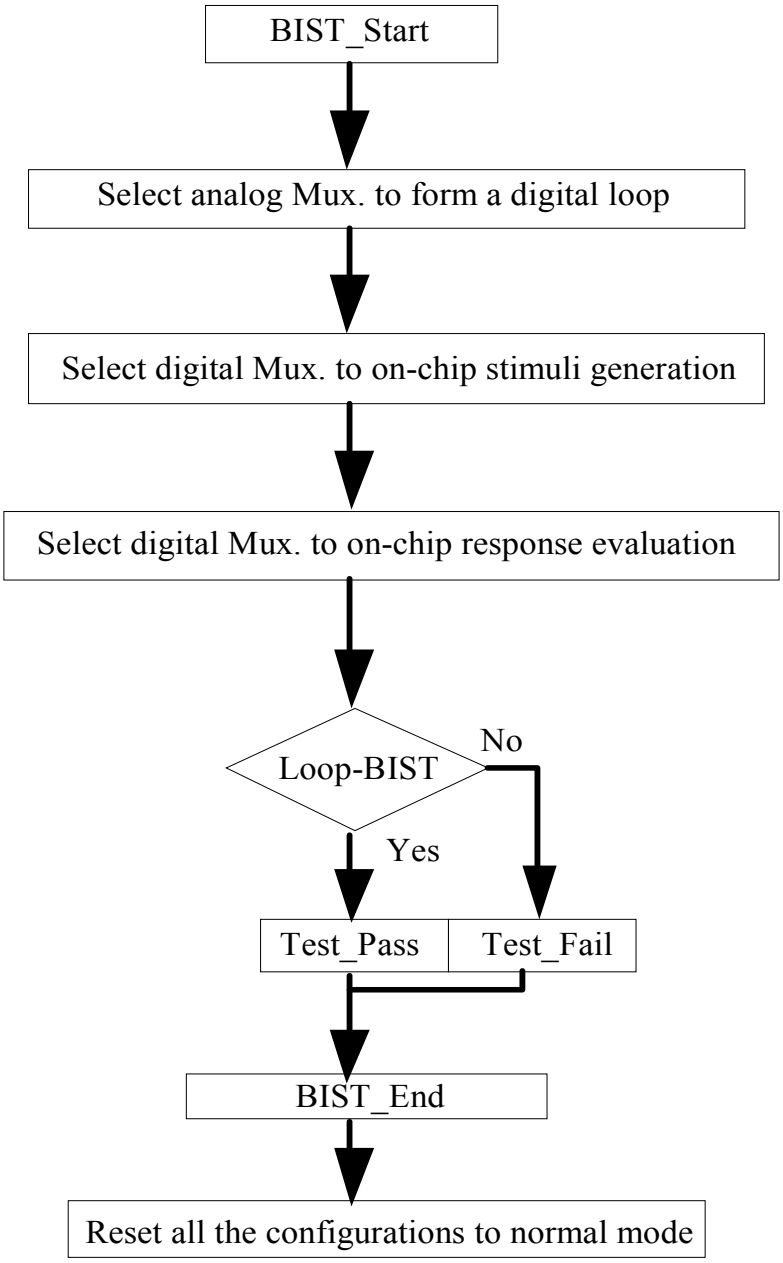

Fig. 3.9: Algorithm of loop BIST

Chapter 4

Wave Digital Filter

Wave-digital filter, in the literature abbreviated as WDF, was first introduced by A. Fettweis in the early 1970s [64]. WDF is originally conceived as a way of discretizing analog filter containing lumped components. The various studies about WDF have revealed remarkable characteristics: WDF displays low sensitivity to coefficients, it can allow multiplier-free signal processing, and limit-cycle oscillations can be kept under control. All of these lead to considerable savings on hardware overhead without loss in its performance.

Moreover, in [65], L. Gaszi has derived and listed top-down design steps, which gives a big aid to the designers. In this chapter, the generic topic of filter design will be reviewed firstly, and then it will be explained why WDF, in particular the category of lattice WDF, is so convenient.

4.1 Classical filter design

It is well known that an analog filter can be converted into the digital domain through a so-called bilinear transformation [63]:

$$s = \frac{2}{T}\frac{z-1}{z+1} \tag{4.1}$$

because this transformation preserves stability and energetic properties: $\mathrm{Re}\{s\} < 0 \Leftrightarrow |z| < 1$. This approach corresponds to approximating continuous time integration with the trapezoid method of numerical integration.

In fact, the obtained filter is a numerical integration scheme for the system which describes the time evolution of the analog network.

If the sampling time is denoted by T, and the analog frequency in the analog domain by Ω and its corresponding digital frequency by ω, two equations can be obtained: $s = j\Omega$ and $z = e^{jwT}$. Then Ω can be derived through the bilinear transform:

$$\Omega = \frac{2}{T}\tan\frac{\omega T}{2} \tag{4.2}$$

This corresponds to a compression of the frequency axis as $\Omega : 0 \to \infty$ is mapped to $\omega : 0 \to \pi f_s$. Due to the tangent function, this compressed range is then periodically repeated with period $2\pi / T$. A direct consequence is that sharpness of the transition band increases as compared to the original frequency response, which implies that the given tolerance scheme could be satisfied with a lower filter order. The closer the transition band is to the Nyquist frequency, the more extreme the compression becomes (and thus the higher the saving in terms of filter order). As mentioned, a convenient realization is through wave digital filter, which will be introduced throughout this chapter.

4.2 The principles of Wave Digital Filter (WDF)

The structures of wave digital filter are obtained from classical LC and microwave filter networks, so that each WDF has a corresponding reference filter in the analog domain. WDF actually consists of numerous subfamilies, many with equivalent linear behavior, among which the designer can choose the one that exhibits the best nonlinear behavior (consequences of quantization noise, round-off noise, saturation etc.). In particular, it can be seen that the category of WDF based on passive, lattice model networks presents several advantages, which is also adopted in this work.

4.2.1 Derivation of WDF

The essential difference of WDF technique to other filter design approaches is the

choice of the physical quantities used to represent the signals. Instead of the typical voltage and current, wave quantities borrowed from line theory are used, which is also the reason that such filter is named wave digital filter. Lumped elements in circuits (capacitors, inductors, resistances, sources, ideal transformers, gyrators, circulators. . .) can all be represented through voltage and current or also through incident and reflected voltage waves and, consequently, have a wave digital equivalent. While this is merely a change of variables, it has the advantage of delivering an alternative description of the dynamic behavior of the network: energy incident on a circuit element may be reflected back through the same port, or transmitted through to a different port. The incident, reflected and transmitted energies are carried by waves.

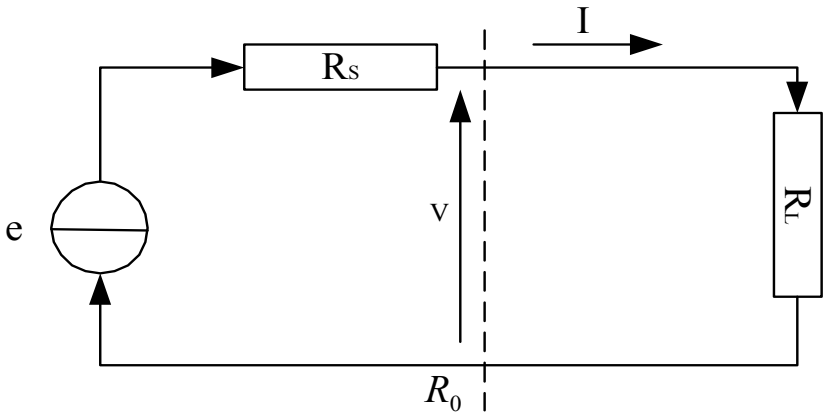

Fig. 4.1: Transmission line for the derivation of wave quantities

Not only the single elements but also the interconnections have to be converted. The resulting net consisting of adders, sign inverters and multipliers is called adaptor, and it is a series adaptor or a parallel adaptor according to whether it simulates a series or a parallel connection. Finally, elements and adaptors are connected to shape the resulting filter. The choice of traveling waves as signal representatives derives from the need of satisfying the following conditions of any signal flow-graph [64]:

1. An ordered sequence of operations to be performed must be identifiable.

2. All such operations must recur with frequency $f_s = 1/T$ or its multiples.

These conditions have direct implications in that: 1) no delay-free loops are allowed, otherwise condition 1 is violated; 2) a total loop delay must be a multiple of the working period, otherwise condition 2 is violated. Fettweis also showed that this approach not only results in realizable systems, but also leads to filters in which both stability and passivity can be guaranteed even after the quantizing operations are taken into ac-

count [64]. Wave variables have their origin in transmission line theory. Consider the terminated line of characteristic impedance R_0 in Fig. 4.1. The voltage (or current) at any position is assumed to be composed of an incident voltage wave V^+ traveling from source to load and a reflected voltage wave V^- traveling from load to source. Then:

$$\begin{cases} V = V^+ + V^- \\ I = I^+ + I^- \end{cases} \tag{4.3}$$

By definition, the incident A_n and reflected B_n traveling waves at port n (n= {1, 2}) are a linear transformation of the voltage V_n and current I_n at the same port:

$$\begin{cases} A_n(s) = V_n(s) + R_n I_n(s) \\ B_n(s) = V_n(s) - R_n I_n(s) \end{cases} \tag{4.4}$$

where in physical systems R_n is the port resistance; if the length of the line is reduced until it is infinitesimal, R_n can be arbitrarily chosen, while the pair A_n and B_n describe the electrical state of the *n*-th port, just like V_n and I_n.

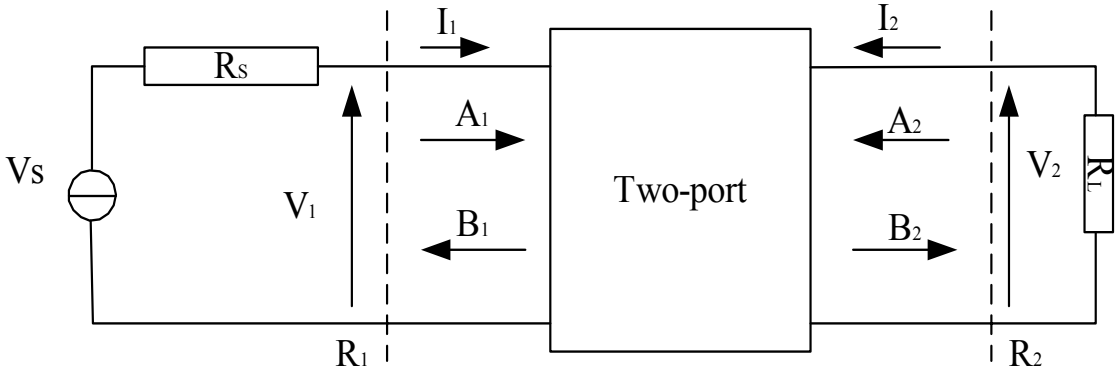

Fig. 4.2: Doubly-terminated two-port network

If we now substitute the transmission line with a generic two-port whose transfer function is $H(s)$, we obtain a doubly resistively terminated network illustrated in Fig 4.2, through which it can be derived by some mathematical deduction due to the linear system theory [66]:

$$\begin{cases} A_1 = V_s \\ B_1 = 2V_1 - V_s \end{cases} \quad \text{and} \quad \begin{cases} A_2 = 0 \\ B_2 = 2V_2 \end{cases} \tag{4.5}$$

From line theory the so-called scattering matrix [*S*] can be derived, which linearly reflects the vector of the incident waves $\vec{A} = (A_1, A_2, \ldots)^T$ to that of reflected waves $\vec{B} = (B_1, B_2, \ldots)^T$ by $\vec{B} = [S]\,\vec{A}$ and whose generic element is defined as:

$$S_{ji} = \frac{B_j}{A_i}, \quad (A_{k \neq i} = 0) \tag{4.6}$$

it can be obtained obviously:

$$S_{21}(s) = \left.\frac{B_2}{A_1}\right|_{A2=0} = 2\frac{V_2}{V_s} = 2H(s) \tag{4.7}$$

That means both signal variables can be equivalently employed to describe electronic network. Such equivalent relationship is illustrated in Fig. 4.3.

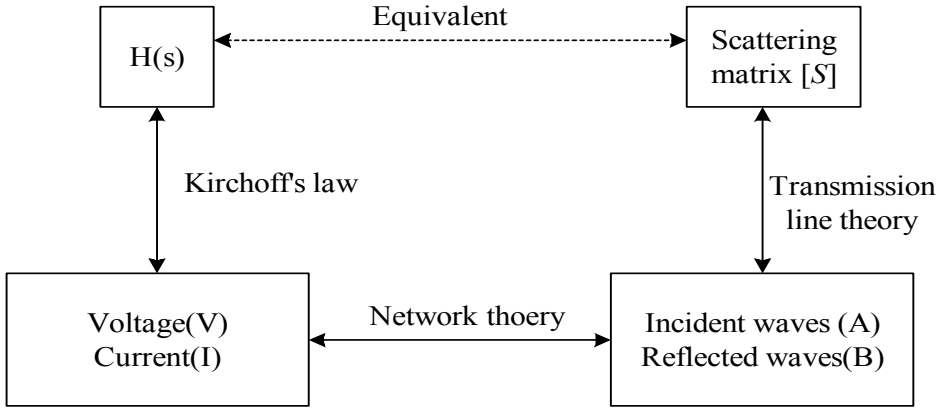

Fig. 4.3: Relationship between H(s) and [*S*]

4.2.2 Derivation of wave flow diagrams

As mentioned, the sources, elements and interconnections of the reference filter have to be replaced by their wave digital equivalents to shape a wave- flow diagram or a signal flow-graph representing the scattering variables as signals.

Firstly, let us consider the most convenient case for RLC-WDF – one port network as

in Fig. 4.4. In general the transfer function of one-port network is expressed by the reflection factor $S = B/A$, the port impedance R_p and the input impedance $Z = V/I$ as:

$$S(\psi) = \frac{B(\psi)}{A(\psi)} = \frac{V(\psi) - R_p I(\psi)}{V(\psi) + R_p I(\psi)} = \frac{Z(\psi) - R_p}{Z(\psi) + R_p} \tag{4.8}$$

if the complex frequency ψ defined as $\psi = \tanh(sT/2)$ is introduced, where the definitions of s and T are the same as those of the equation (4.2).

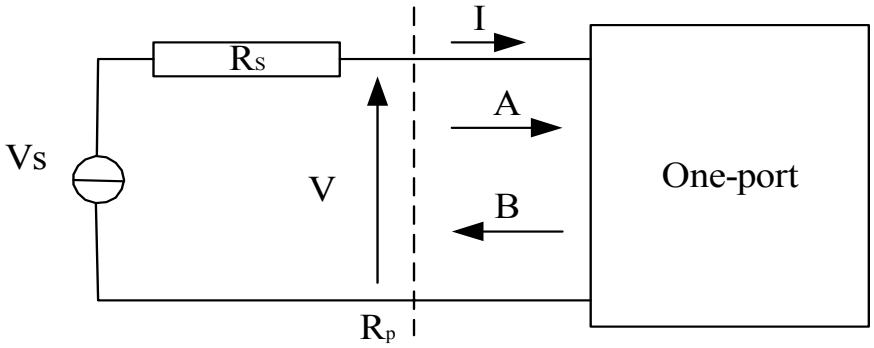

Fig. 4.4: One-port network

$Z = j\phi L$ can be inserted in the equation (4.8) to derive the wave digital inductor. With the further assumption $R_p = L$, a simple structure can be obtained:

$$S(j\phi) = \frac{j\phi - 1}{j\phi + 1} \quad \rightarrow \quad -z^{-1} \tag{4.9}$$

which means the wave-digital inductor results simply to be a negative delay. In fact, all elementary circuit components can be derived in the same way. The wave-digital conductors of some commonly used elementary circuits are listed as follows:

Inductance L

$$\begin{aligned} Z_L(j\phi) &= j\phi L \\ S_L(j\phi) &= \frac{j\phi L - R_p}{j\phi L + R_p} = -\frac{1 - j\phi}{1 + j\phi}\bigg|_{R_p = L} = -z^{-1} \\ B_n &= -A_{n-1} \end{aligned} \tag{4.10}$$

Capacitance C

$$\begin{aligned} Z_C(j\phi) &= C / j\phi \\ S_C(j\phi) &= \frac{C / j\phi - R_p}{C / j\phi + R_p} = \left.\frac{1 - j\phi}{1 + j\phi}\right|_{R_p = 1/C} = z^{-1} \\ B_n &= A_{n-1} \end{aligned} \tag{4.11}$$

Resistance R

$$\begin{aligned} Z_R(j\phi) &= R \\ S_R(j\phi) &= \frac{R - R_p}{R + R_p} = 0\Big|_{R_p = R} \\ B_n &= 0 \end{aligned} \tag{4.12}$$

Short-circuit

$$\begin{aligned} Z_S(j\phi) &= 0 \\ S_S(j\phi) &= \frac{0 - R_p}{0 + R_p} = -1\Big|_{\forall R_p} \\ B_n &= -A_n \end{aligned} \tag{4.13}$$

Open-circuit

$$\begin{aligned} Z_O(j\phi) &\to \infty \\ S_C(j\phi) &\to \frac{\infty - R_p}{\infty + R_p} = 1\Big|_{\forall R_p} \\ B_n &= A_n \end{aligned} \tag{4.14}$$

Resistive voltage source

$$\begin{aligned} V(j\phi) &= E(j\phi) + I(j\phi)R_s \\ B(j\phi) &= E(j\phi)\frac{2R_p}{R_s + R_p} + A(j\phi)\frac{R_s - R_p}{R_s + R_p} = E(j\phi)\Big|_{R_p = R_S} \end{aligned} \tag{4.15}$$

It should be noted that wave variables corresponding to different ports are scaled by different port resistances, so the wave- flow diagrams obtained from the relative one-ports cannot be just connected. From a transmission line perspective, this is equivalent to saying that whenever there is an impedance change, reflection and transmission are expected to take place to satisfy continuity requirements:

$$\sum_{i=1}^{n} \frac{v_i^{+}(t)}{R_i} = \sum_{i=1}^{n} \frac{v_i^{-}(t)}{R_i} \tag{4.16}$$

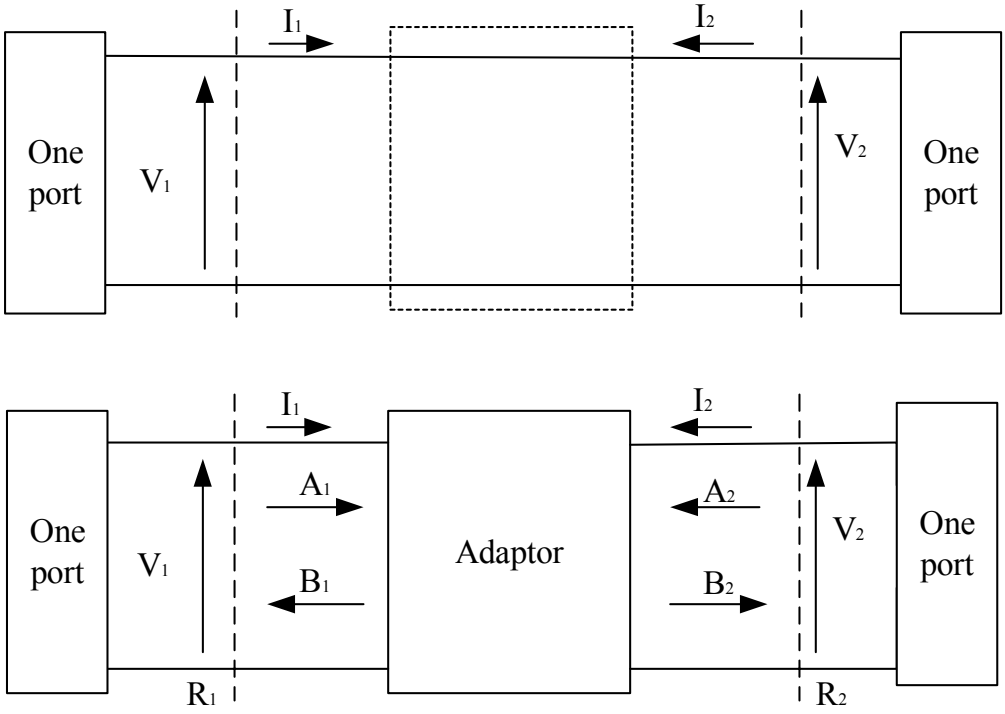

Fig. 4.5: Voltage divider a) classical filter; b) WDF with adaptor

In other words, the wave impedances have to be adapted by the adaptor in the ports. Here a particularly common case: two-port adaptors, because they are most economical to realize. As an example, consider a two-port network which serves as a voltage divider illustrated in Fig. 4.5, which leads to:

$$\begin{cases} V_1 = V_2 \\ I_1 = -I_2 \end{cases} \rightarrow \begin{cases} A_1 + B_1 = A_2 + B_2 \\ (A_1 - B_1)/R_1 = (B_2 - A_2)/R_2 \end{cases} \tag{4.17}$$

With elaborating the equations, there will be:

$$\begin{cases} B_1 = \dfrac{R_2 - R_1}{R_2 + R_1} A_1 + \dfrac{2R_1}{R_2 + R_1} A_2 \\ B_2 = \dfrac{2R_2}{R_2 + R_1} A_1 + \dfrac{R_2 - R_1}{R_2 + R_1} A_2 \end{cases} \tag{4.18}$$

which can be expressed in the form of matrix:

$$[B] = \begin{pmatrix} -\gamma & 1+\gamma \\ 1-\gamma & \gamma \end{pmatrix} \cdot [A] \tag{4.19}$$

where $[A] = (A_1, A_2)^T$, $[B] = (B_1, B_2)^T$ and $\gamma = (R_1 - R_2)/(R_1 + R_2)$. Obviously, the vector of incident wave $\overline{A}$ is related to that of reflected wave $\overline{B}$ by a matrix with the parameter of γ. This matrix is the scattering matrix [*S*] of this two-port network and, of course, also the adaptor between the two one-port networks.

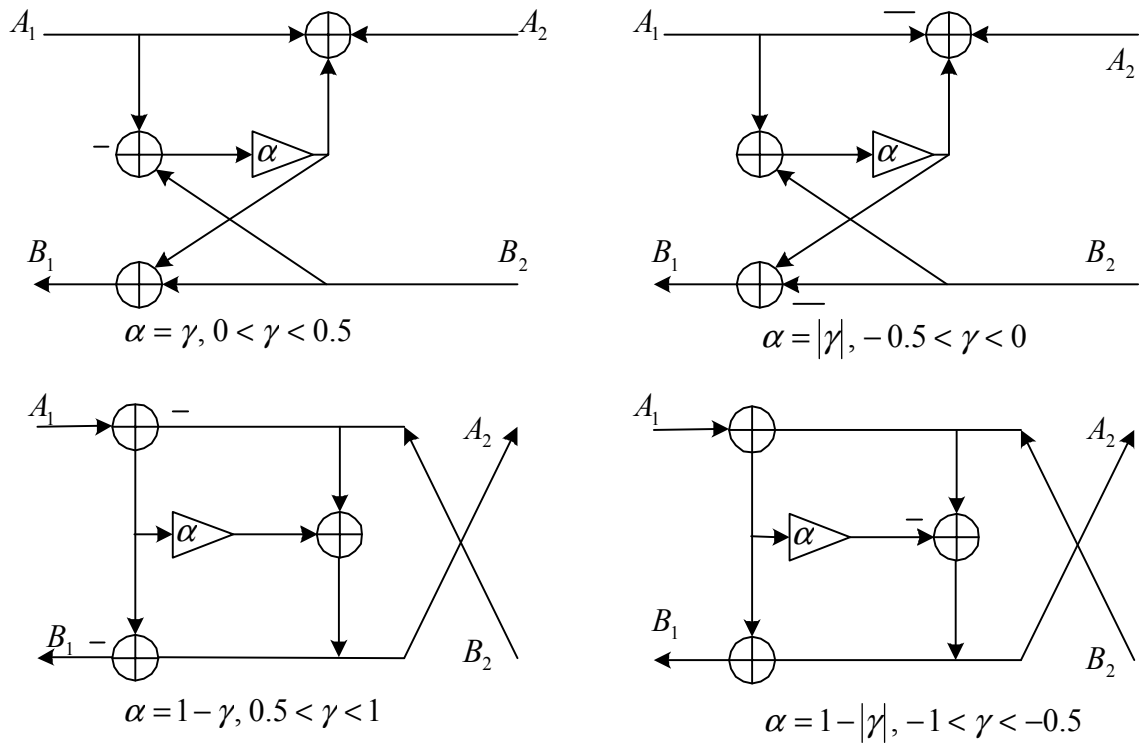

Fig. 4.6: Two-port adaptor types optimized for sinusoidal input

The resulting two-port adaptors need only one multiplier γ of modulus $|\gamma| < 1$. A simple manipulation can be used to convert the coefficient γ into a positive α of modulus $|\alpha| < 1/2$, if four cases are distinguished. Consequently, four adaptor types will result as illustrated in Fig. 5.6, which provides the best scaling for sinusoidal input. The rea-

son of reducing the coefficients from γ to α is that it allows the prevention of over flow non-linearity because it scales the signal internally.

For a generic n-port network, the adaptor should also have n port. Then there are two types of the adaptor: parallel adaptor and series adaptor, according to the different connected behavior of electrical quantities such as voltage and current at ports. Because only the two-port adaptors are employed to form the WDF in this work, the detail information about the parallel adaptors and series ones will not be further introduced in this dissertation. Such information can be found in [64] [65] [67] [68] [70].

4.3 Lattice WDF

As well known, passive LC-filters in ladder configuration would lead to WDF needing three-port adaptors, and they have been proven uneconomic as the number of elements needed to realize them exceeds that of classical filters [64] [65]. In contrast, WDF derived from lattice LC references require two-port adaptors, which need only a single coefficient performing the adaptation and an overall number of multipliers equal to the filter degree.

When two-port adaptors are connected to a delay element as in Fig. 4.7(a), a first order all-pass transfer function with respect to the input A_1 and the output B_1 results

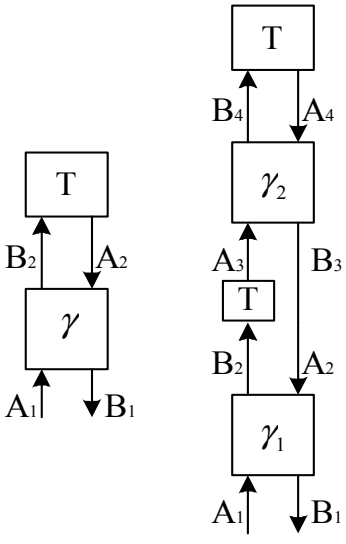

Fig. 4.7: All-pass section for lattice WDF (a) first order; (b) second order

$$H(z) = S_{11}(z) = \frac{B_1(z)}{A_1(z)} = \frac{(1-\gamma z)}{(z-\gamma)} \tag{4.20}$$

When two adaptors are connected like shown in Fig. 4.7(b), a second order all-pass section results

$$H(z) = S_{11}(z) = \frac{B_1(z)}{A_1(z)} = \frac{1+(\gamma_1-1)\gamma_2 z - \gamma_1 z^2}{-\gamma_1+(\gamma_1-1)\gamma_2 z - z^2} \tag{4.21}$$

These results have a very important characteristic -- the numerator and denominator have mirrored hermitical coefficients, which imply conjugate reciprocal zero-pole pairs [69]. This means that the all-pass behavior is unaffected by quantization, because the symmetry in the coefficients doesn't depend on the particular value they assume. Moreover, stability is guaranteed as long as $|\gamma_i| < 1$. The sensitivity of the overall trans-

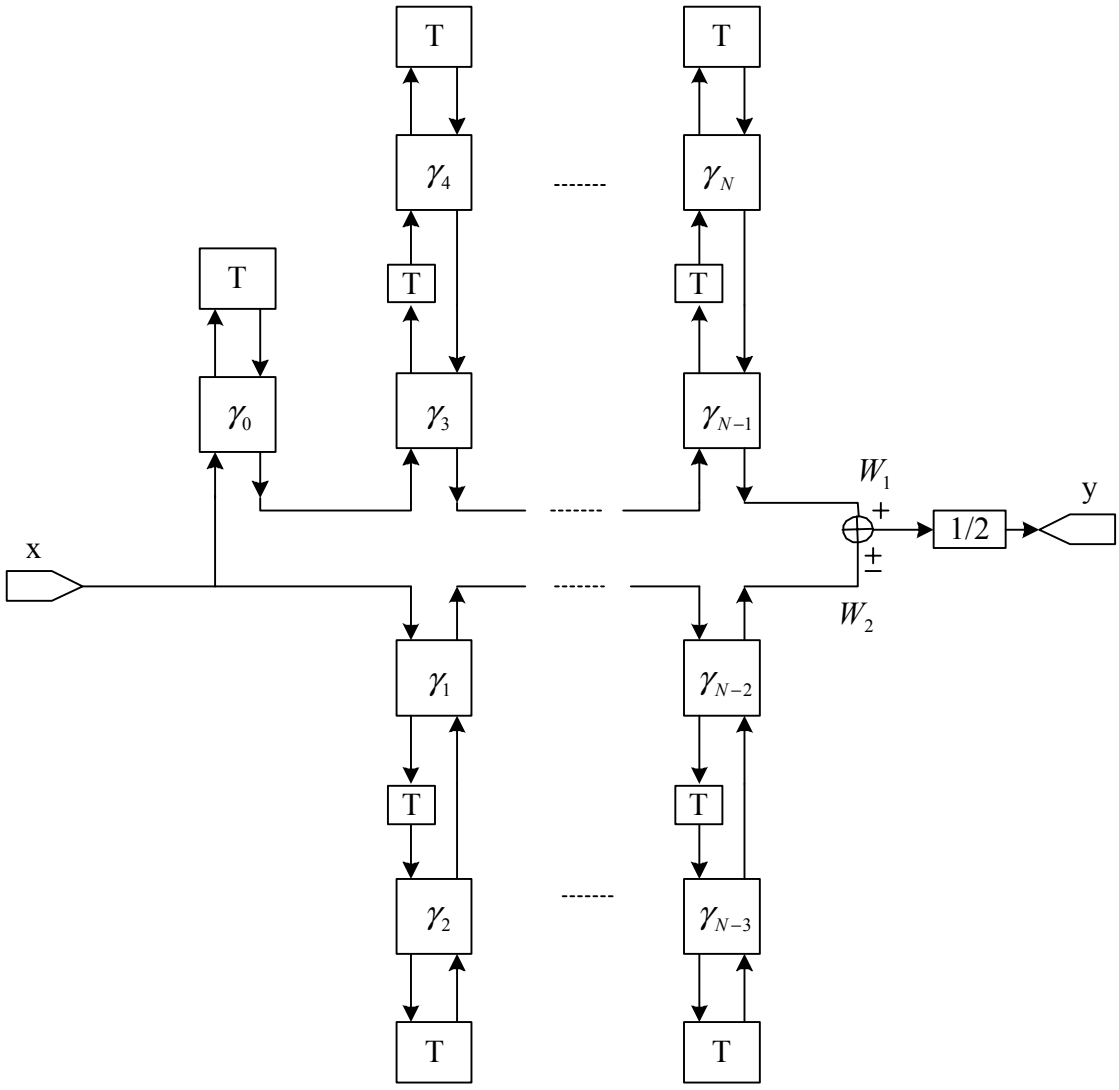

Fig. 4.8: Lattice WDF

fer function to variations of the γ_i's is low, which allows these to be represented with a considerably smaller word-length than with direct realizations.An *N*th degree lattice WDF is created by cascading low-order all-pass transfer functions to form two (all-pass) branches, which is illustrated in Fig. 4.8. Since for achieving low-sensitivity in the pass-band *N* must be odd [70], these consist of one first order section and *(N-1)/2* times of second order sections. The overall transfer function is given by

$$H(z)=\frac{1}{2}\left(H_1(z)\pm H_2(z)\right) \tag{4.22}$$

where

$$\begin{aligned} H_1(z)&=\frac{W_1(z)}{X(z)}=\frac{1-\gamma_0 z}{z-\gamma_0}\prod_i \frac{1-(1-\gamma_i)\gamma_{i+1}z-\gamma_i z^2}{-\gamma_i-(1-\gamma_i)\gamma_{i+1}z-z^2} \\ H_2(z)&=\frac{W_2(z)}{X(z)}=\prod_i \frac{1-(1-\gamma_i)\gamma_{i+1}z-\gamma_i z^2}{-\gamma_i-(1-\gamma_i)\gamma_{i+1}z-z^2} \end{aligned} \tag{4.23}$$

From the equation (4.22), a conclusion can be easily drawn that two complementary filters can be generated from the same hardware by respectively adding or subtracting the two branches. For example, a low-pass and a high-pass with the same corner frequency, or a pass-band and a stop-band.

Now consider a lossless, doubly-terminated symmetrical lattice two-port as in Fig. 4.9, which is considerably difficult to be realized in the analog domain, because the tolerances and drifts typical of this type of circuits cause the impedances often not to have equal value. However, the determinism of digital circuits lets them be realized more easily. The relationships between voltages and currents are

$$\begin{cases} V_1=\dfrac{Z_2-Z_1}{2}\left(I_1+I_2\right) \\ V_2=\dfrac{Z_2+Z_1}{2}\left(I_1+I_2\right) \end{cases} \tag{4.24}$$

By introducing the reflectance

$$\begin{cases} S_1=\dfrac{Z_1-R}{Z_1+R} \\ S_2=\dfrac{Z_2-R}{Z_2+R} \end{cases} \tag{4.25}$$

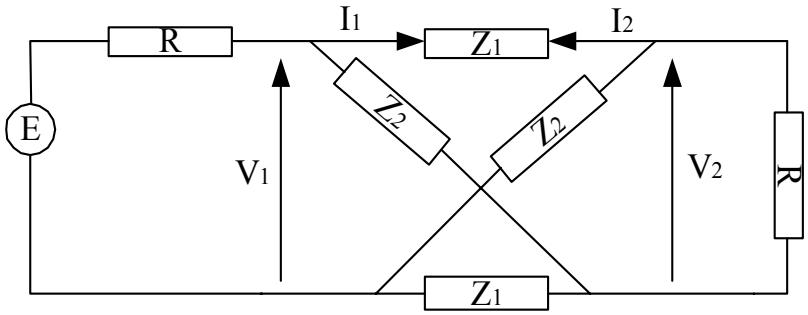

Fig. 4.9: Lattice two-port

and if the impedances $Z_i\ (i=1,2)$ are reactance like capacitors or inductors, the $S_i\ (i=1,2)$ become all-pass functions and can be represented by the branches of a lattice WDF. Fig. 4.10(a) shows a general case of lattice WDF. If only one input and one output are considered, that is only the incident wave at the input terminal $x = A_1$ and the reflected one at the output terminal $y = B_2$, the simplified diagram of Fig. 4.10(b) is obtained, for which

$$S_{21} = \frac{B_2}{A_1} = \frac{S_2 - S_1}{2} \tag{4.26}$$

And there is:

$$\alpha(\omega) = -20\log|S_{21}(j\omega)| \tag{4.27}$$

All-pass functions like S_1 and S_2 can be described by a ratio of polynomials with mirror coefficients in $j\omega$[69], which alternates the sign in ψ. Let $g_i(\psi)$ be a Hurwitz polynomial; then the branches can be described by

$$S_i(\psi) = \frac{g_i(-\psi)}{g_i(\psi)} \tag{4.28}$$

which is a ratio of real polynomials having roots in reciprocal locations. Now, a first order all-pass in the ψ-domain looks like

$$S(\psi) = \frac{d - j\omega}{d + j\omega} = \frac{d - \psi}{d + \psi} \tag{4.29}$$

Convert it to the z - domain using the bilinear transform, which gives:

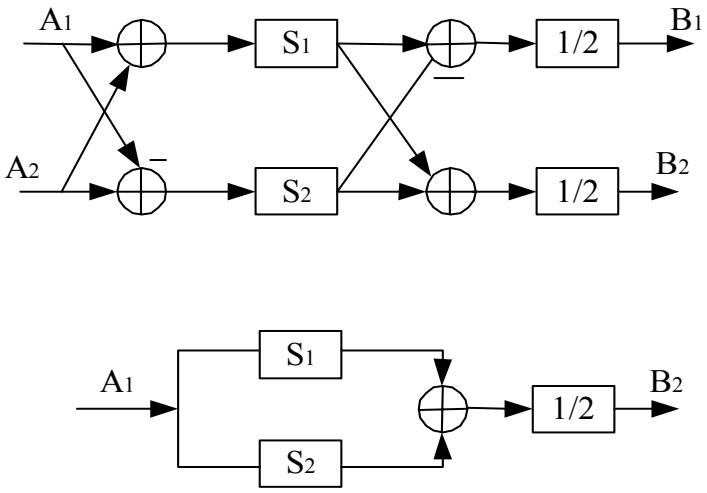

Fig. 4.10: WDF obtained from lattice reference filter (a) as a two-port;
(b) when only one input and one output are considered Lattice two-port

$$S(\psi)=\frac{d\left(1+z^{-1}\right)-\left(1-z^{-1}\right)}{d\left(1+z^{-1}\right)+\left(1-z^{-1}\right)}=\frac{z^{-1}-\dfrac{1-d}{1+d}}{1-z^{-1}\dfrac{1-d}{1+d}} \tag{4.30}$$

so that the corresponding first order wave digital all-pass filter (see Fig. 4.7) has a two-port adaptor of coefficient

$$\gamma=\frac{1-d}{1+d} \tag{4.31}$$

Similarly, the corresponding adaptor coefficients of a second order reflectance looks like $S(\psi)=\left(\psi^2-c\psi+d\right)/\left(\psi^2+c\psi+d\right)$ can be expressed as:

$$\begin{cases}\gamma_1=\dfrac{c-1-d}{c+1+d}\\ \gamma_2=\dfrac{1-d}{1+d}\end{cases} \tag{4.32}$$

In all cases there is $|\gamma_i|$ <1 so that stability is ensured. For an *N*th order filter with coefficients $(\gamma_0,\gamma_1,...,\gamma_N)$, the overall transfer function is then:

$$H(\psi)=\frac{1}{2}\left(S_1(\psi)\pm S_2(\psi)\right)=\frac{f(\psi)}{g(\psi)} \tag{4.33}$$

which follows

$$g(\psi) = g_1(\psi)\, g_2(\psi) = (\psi + b_0) \prod_{i=1}^{(N-1)/2} \left(\psi^2 + c_i \psi + d_i\right) \tag{4.34}$$

where the denominator of the polynomials defines the position of the filter poles. Therefore, the filter is built by first positioning the poles of the desired transfer function, then those of the zeros are found. In [70] the design for the single cases of Butterworth, Chebychev and Cauer filter types are introduced in details.

Chapter 5

On-Chip Signal Generation

The on-chip signal generator provides the testing stimulus for the loop-BIST, and for the eventual ADC-BIST and DAC-BIST. This means that there are two types of signal generator: analog signal generator and digital signal generator. A sinusoidal input is commonly used as the testing stimulus by the production test, because it can verify both the magnitude and the phase of an output signal as function of the input frequency; moreover, it can quantify the extent of nonlinearity in an output by comparing the power contained in the harmonics or noise to that of the fundamental signal, referred to as signal-to-noise ratio (SNR) or signal-to-noise-and-distortion ratio (SNDR) [63]. Because the studied cases in the following chapters are mainly concerned with the codec chips, the frequency of the testing stimulus is 1 kHz. But it should be noted that the signal generation algorithm introduced in this chapter has a very wide frequency range and is not limited only to 1 kHz.

Furthermore, the reason for choosing a 1 kHz sinusoidal waveform as the testing stimulus for the codec chips is that one particular frequency has to be elected to represent the whole band. Concerned with voice-band signals due to the speech processing character of the circuit under test (CUT), it seems sensible to consider the ear's sensitivity to the different frequencies recommendations advice for telephone signals. The human ear is modeled with a so-called psophometrics filter in Europe or C-MESSAGE filter in North America, illustrated in recommendations G.714 and O.413, which treat the signal's components according to the perception of sounds. Both filters display a maximum at about f = 1000 Hz and makes this frequency the most delicate and significant tone. Therefore, a choice falling in a neighborhood of 1 KHz appears reasonable.

In this chapter, some digital sinusoidal waveform generation methods are introduced

as well as their principles, advantages and disadvantages. An analog sinusoidal signal is able to be obtained easily by feeding such digital sinusoidal waveform through a DAC. A direct analog method for generating an analog sinusoidal stimulus on chip is provided at the end of this chapter, which is based on the Delta-Sigma (DS) modulation technique and leads to a design flexibility when embedded in the BIST design.

5.1 ROM look-up tables

One idea is to store the values of a sampled sinusoidal waveform in a Read-Only Memory (ROM) Look Up Table (LUT) [99]. Due to the symmetries of the signal considered, it could be sufficient to store the values belonging to one quadrant. The further method to decrease the number of samples, or equivalently the size of the memory, is the usage of interpolation technique. Interpolation or trigonometric identifiers are used to compute the sample lying between two stored ones. Obviously, the more samples there are, the larger the ROM and the lower the order of the interpolation filter will be. A trade-off has to be drawn between the memory size and the processing time increase due to the growing complexity. By the ROM look-up table method, there are two ways to change the output frequency of the generated signal: 1) use the address counter with variable clock frequency; 2) use address adder with fixed clock frequency. Both cases are illustrated in Fig. 5.1, where CTR means the Address Counter Register and REG means Register. The maximum clock frequency in both cases is determined by the limited accessing rate of ROM.

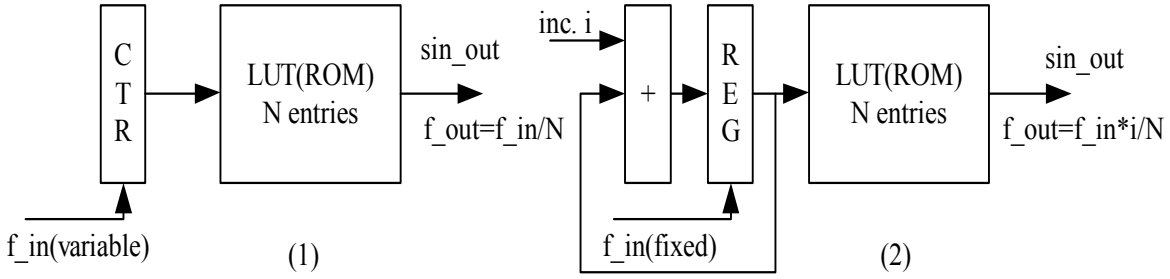

Fig. 5.1: Two approaches for changing the output frequency: (1) variable frequency (2) fixed clock.

A memory containing N n-bit words has $N \cdot n$ elementary cells (bits). N cannot be reduced too much because it sets the periodicity of the output samples and, accordingly, that of the quantization error. To compute a sinusoidal waveform with the high resolution above 14 bits, the required resource gives an order of magnitude of hundreds *k*Bits.

Even if some logic could reduce this figure by more than half, it still remains too large to be accepted by the BIST application. This does not even include the access procedures, control logic and redundant cells that a memory must have. Moreover, it is recognized that memories are often responsible for a lower yield and would cause the number of faulty chips to increase.

5.2 Recursive evaluation

Another approach involves constructing an oscillator through a recursive filter system, whose poles lie on the unit circle [66] [100] [101]. Let T be the sampling period, $f_s = 1/T$ the sampling frequency and $\omega_0 = 2\pi f_0$ the pulsation of the sinusoidal waveform. Then the sequence to be generated is

$$h[n] = \cos(\omega_0 T n)\, u[n] \tag{5.1}$$

where $u[n]$ representing the unit step. Then, its Z-transform

$$h[z] = \frac{1 - z^{-1}\cos(\omega_0 T)}{1 - 2z^{-1}\cos(\omega_0 T) + z^{-2}} \tag{5.2}$$

can be implemented through a 2nd order IIR filter, as shown in Fig. 5.2, whose output will be a (co)sinusoidal wave when excited by a Dirac-pulse. And parameter b is defined as $b = 2\cos(\omega_0 T)$. Then the time-domain equation is obtained:

$$y[n] = by[n-1] - y[n-2] + x[n] - (b/2)x[n-1] \tag{5.3}$$

It would clearly be equally possible to generate a sinusoidal signal instead of a cosine

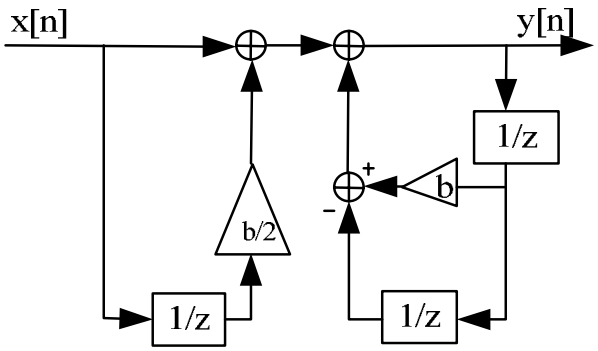

Fig. 5.2: Block scheme of 2nd order recursive oscillator

wave. But the latter is preferred because of the simpler coefficients involved. The Z-Transform of $h[n]=\sin(\omega_0 Tn)\,u[n]$ is

$$h[z]=\frac{1-z^{-1}\sin(\omega_0 T)}{1-2z^{-1}\cos(\omega_0 T)+z^{-2}} \tag{5.4}$$

where a second coefficient appears, namely $a=\sin(\omega_0 T)=\sqrt{1-(b/2)^2}$, which is not linearly related to *b* and complicates the implementation with an additional multiplication. This IIR filter, as a second order filter, can preserve only two states at a time. And it has a pulse input only one non-zero entry. Therefore, an adder can be prevented by setting appropriate initial conditions and eliminating the input signal completely. In this case the time-domain representation becomes:

$$\begin{cases} y[n]=by[n-1]-y[n-2], & n\geq 0 \\ y[-1]=1 \\ y[-2]=b/2 \end{cases} \tag{5.5}$$

which means that the forced evolution of the system have been suppressed, i.e. the part steered by the input, and let the system follow only its free evolution, or, in other words, the part set by the initial states' conditions [66]. The corresponding scheme is represented in Fig. 5.3.

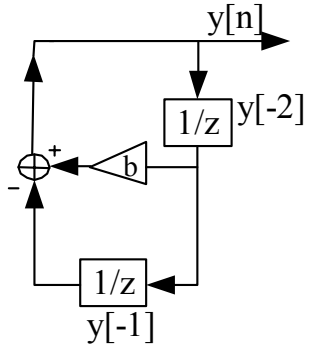

Fig. 5.3: 2nd order oscillator with zero-input

Now let us take into account the effects of quantization of the coefficients (in this case only *b*) and of the signal samples. If *b′* is an approximation of *b* expressed as finite sum of powers of 2

$$b\rightarrow b'=\sum_{i=p1}^{p2} c_i 2^{-i} \quad c_i\in\{0,1\} \tag{5.6}$$

this inevitably results in a change of the generated frequency, which gives

$$f_0 \rightarrow f_0' = \frac{f_s}{2\pi} \arccos \frac{b'}{2} \tag{5.7}$$

Coefficient quantization causes a variation in the position of the zeros and poles of a system. The pole radius of the oscillating system is unaffected by quantization, as it is fixed to 1. The poles move and remain on the unit circle, so that the amplitude of the signal neither decreases nor increases over time. Thus the filter is still stable. The reference wave becomes:

$$y[n] \rightarrow y[n]' = \cos\left(2\pi\, n \frac{f_0'}{f_s}\right) u[n] \tag{5.8}$$

The resolution of this approach is limited by the word length of the system [66] [100] [101]. This algorithm is unable to be implemented under fixed-point system. An additional risk is that if some uncontrollable events (for example, external physical perturbations) cause one single value to be wrong, all successive values would become fallacious. The algorithm will never recover. The reason is that the system has only a free evolution, as its input has been set to zero, and there is no direct control over the states' values.

5.3 COordinate Rotation DIgital Computer (CORDIC) algorithm

The Coordinate Rotation Digital Computer (CORDIC) algorithm can be used for fast computations of trigonometric functions and their inverses, multiplication/division, as well as for conversion between binary and mixed radix number systems [102] [103] [104]. The CORDIC method evaluates elementary functions merely by look-up-table (LUT), shift and add operations. A small number (of the order of n, where *n* bits of precision is required in the evaluation of the functions) of pre-calculated fixed constants is required to be stored in the look-up table.

The CORDIC algorithm has nice geometrical interpretations [102] [103]: trigonometric, exponential, multiply functions are evaluated via rotations in the circular, hyperbolic and linear coordinate systems, respectively. Their inverses (i.e., inverse trigonometric functions, logarithm and division) can be implemented in a "vectoring" mode in the appropriate coordinate system. The principle and the technical detail of producing

a sinusoidal waveform signal with CORDIC algorithm can be found in [102] – [107], which are summarized in the following.

The rotation of a vector by angle θ can be expressed by a transform from (x_0, y_0) to (x_1, y_1) in Cartesian coordinates, which is given by the operation [109]:

$$\begin{cases} x_1 = x_0 \cos\theta - y_0 \sin\theta \\ y_1 = x_0 \sin\theta + y_0 \cos\theta \end{cases} \rightarrow \begin{cases} x_1 = \cos\theta(x_0 - y_0 \tan\theta) \\ y_1 = \cos\theta(x_0 \tan\theta + y_0) \end{cases} \tag{5.9}$$

In the CORDIC method, the rotation by an angle θ is implemented as an iterative process. Such process consists of micro-rotations during which the initial vector is rotated by pre-determined step angles θ_i. Any angle θ can be represented to certain accuracy by a set of n step angles θ_i. Given a direction of rotation or sign σ_i, the angle θ can be approximated by the sum of the step angles θ_i as follows:

$$\theta = \sum_{i=0}^{n} \theta_i \sigma_i \qquad \sigma_i = [-1, +1] \tag{5.10}$$

The sign of the step angles is determined by the difference between the angle θ and the partial sum of step angle $\theta - \sum_{i=0}^{n} \theta_i \sigma_i$. An auxiliary variable Z_i is introduced that contains the accumulated partial sum of step angles and is used to determine the sign of the next micro-rotation. To simplify the computation, the step angles θ_i are chosen so that $\tan\theta_i$ represents a series of powers of 2: $\tan\theta_i = 2^{-i}$, $i = 0,1,...n$.

The CORDIC method can be employed in two different modes: the “rotation” mode and the “vectoring “mode. In the rotation mode, the co-ordinate components of a vector and an angle of rotation are given and the co-ordinate components of the original vector, after rotation through a given angle, are computed. In the vectoring mode, the co-ordinate components of a vector are given, and then the magnitude and angular argument of the original vector are computed. The rotation mode of the CORDIC algorithm has three inputs, which are initialised to the co-ordinate components of the vector (x_0, y_0), and the angle of rotation $Z_0 = \theta$ and is described by the following iteration equations:

$$\begin{cases} x_{i+1} = x_i - y_i \sigma_i 2^{-i} \\ y_{i+1} = y_i + x_i \sigma_i 2^{-i} \\ Z_{i+1} = Z_i - \sigma_i \arctan 2^{-i} \end{cases} , \sigma_i = \begin{cases} -1, & Z_i < 0 \\ +1, & Z_i > 0 \end{cases} \tag{5.11}$$

A CORDIC micro-rotation is not a pure rotation but a pseudo rotation. A scale factor *K* must be introduced and represents the increase in magnitude of the vector during the rotation process. When the number of iterations (micro-rotations) is fixed, the scale factor is a constant approaching the value of 1.647 as the number of iterations goes to infinity [107]. The elementary functions sine and cosine can be computed using the rotation mode of the CORDIC algorithm if the initial vector is of unit length and is aligned with the abscissa [107].

The CORDIC algorithm can be implemented in hardware using three approaches: a sequential approach – the structure is unfolded in time, a parallel approach – the structure is unfolded in space or a combination of the two. These three approaches and the resulting structures are also referred to in the literature as iterative, cascaded and cascaded fusion. A sequential CORDIC design performs one iteration per clock cycle and consists of three n-bit adders/subtractors, two sign extending shifters, a look-up table (LUT) for the step angle constants and a finite state machine. A parallel CORDIC design is similar to an array multiplier structure consisting of rows of adders/subtractors, with shifts and constants. Parallel CORDIC can be implemented in the form of purely combinational arrays or can be pipelined depending on the size of the design and the requested data rate. A combined CORDIC design is based on a sequential structure where the logic for several successive iterations is cascaded and is executed within one clock cycle [108]. But all the implementations have a common limitation: they must employ ROM to store the predefined value, which is not always available for BIST.

5.4 A new approach -- filtering a periodical signal

5.4.1 Algorithm of filtering a periodical signal

A new method based on filtering a periodical signal is presented in [92] [93]. Every periodic waveform f(x) having a cycle duration T can be represented by a Fourier series [66], which is an infinite sum of sine and cosine waveforms:

$$f(x) = \frac{a_0}{2} + \sum_{k=1}^{\infty}\left(a_k \sin\left(\frac{2\pi kx}{T}\right) + b_k \cos\left(\frac{2\pi kx}{T}\right)\right) \tag{5.13}$$

where

$$
\begin{aligned}
a_k &= \frac{2}{T}\int_0^T \cos\left(\frac{2\pi kx}{T}\right) f(x)\,dx \\
b_k &= \frac{2}{T}\int_0^T \sin\left(\frac{2\pi kx}{T}\right) f(x)\,dx \\
c_k &= \frac{a_k - jb_k}{2}
\end{aligned}
\tag{5.14}
$$

Periodic waveforms such as the rectangular or triangular wave can be readily generated. When such waveforms are positioned on the time axis so as to have even symmetry, the sine coffin's are zero as well as all the $a_k = 0$ for even k. This means that the spectra contain only odd harmonics. When a filter is used to attenuate higher harmonics, a sinusoidal waveform with the same period as the square (or triangle) wave will be obtained at the output. Furthermore, with the computation of the discrete spectra of rectangular and triangular waveform:

$$
\begin{aligned}
a_{k,rect} &= \frac{4M}{kT}\sin\left(\frac{k\pi}{kT}\right) \Rightarrow \left|a_{k,rect}\right| = \frac{4M}{KT} \\
a_{k,trian} &= \frac{2M}{k^2\pi^2}\left[1-(-1)^k\right] \Rightarrow \left|a_{k,trian}\right| = \frac{2M}{k^2\pi^2}
\end{aligned}
\tag{5.15}
$$

where M is referred as the amplitude of the waveform, we can conclude that a triangular input looks preferable because the undesired signal components attenuate more rapidly.

A triangular wave is a particular case of a trapezium wave and that a trapezium can be obtained from a triangular by leveling off the peaks. The spectral components remain the same, but the amplitude of certain a_k can be controlled by the saturation level S ($S < M$ or $S = M$, obviously when $S = M$, the trapezoid waveform returns into triangular wave). Computing the Fourier series of trapezoid waveform, the following equation can be obtained:

$$
\begin{aligned}
a_{k,trap} &= \frac{2M}{k^2\pi^2}\left[1-(-1)^k\right]\cos\left(\frac{k\pi}{2}\left(1-\frac{S}{M}\right)\right) \\
\Rightarrow \left|a_{k,trap}\right| &= \frac{4M}{k^2\pi^2}\left|\sin\left(\frac{k\pi}{2}\frac{S}{M}\right)\right|
\end{aligned}
\tag{5.16}
$$

which tells that

$$
a_k = 0 \Leftrightarrow \frac{k\pi}{2}\cdot\frac{S}{M} = n\pi \qquad (n \in Z,\ 2n < k) \tag{5.17}
$$

Some instances are given in Table 5.1 and show that by properly choosing the saturation level S, the third harmonic disappears completely. This leads to a better transition band in the spectra to simplify the design of the low pass filter with large design margin. The block-level structure of the on chip sinusoidal waveform generator is illustrated in Fig. 5.4.

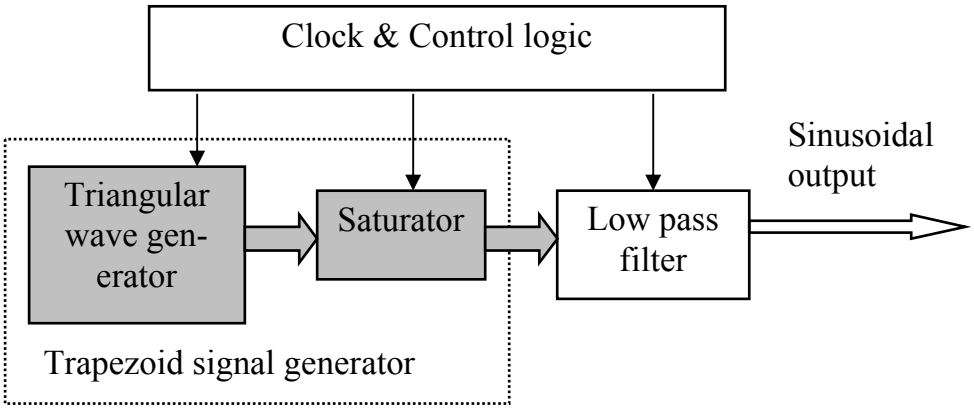

Fig. 5.4: The structure of on chip generator

Table 5.1: n, S and a_k

$a_3 = 0$	$n = 1$	$S = 2/3M$
$a_5 = 0$	$n = 1$	$S = 2/5M$
	$n = 2$	$S = 4/5M$
$a_7 = 0$	$n = 1$	$S = 2/7M$
	$n = 2$	$S = 4/7M$
	$n = 3$	$S = 6/7M$

5.4.2 Generation of the trapezoid waveform

A trapezoid wave can be obtained from a triangular wave by saturating the peaks at a defined level which is indicated as S. A circuit that generates such waves is shown in Fig. 5.5. If the output has n bits, then a counter with modulo 2^{n+1} is used. The two most significant bits (MSBs) are extracted and combined into a controlling signal through a XOR-gate to control a multiplexer. The multiplexer selects the n least significant bits (LSBs) of the counter and their negative. When the controlling signal is high, the direct input is selected. When it is low, the negated input passes.

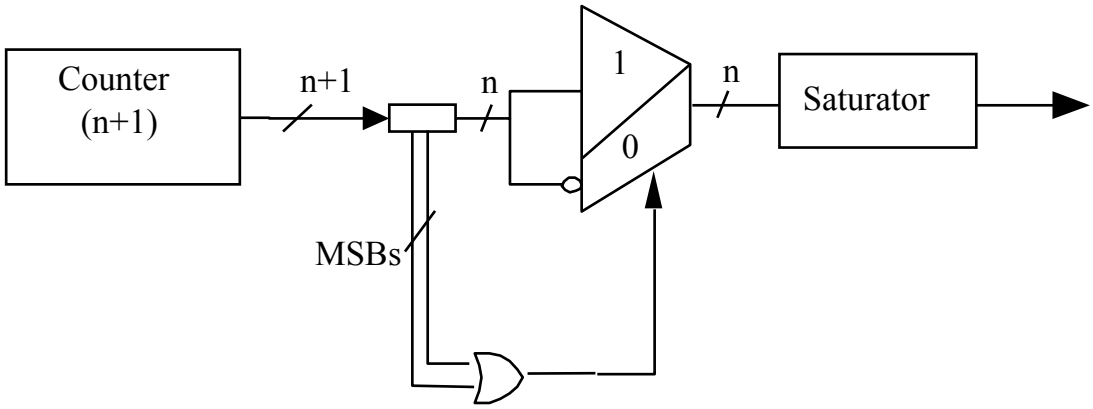

Fig. 5.5: Generation of trapezoid signal

In a two's complement arithmetic, the mentioned waveforms is shown in Fig. 5.6. In the example, a 3-bit triangle is generated with the use of a 4-bit counter. Table 5.2 shows the corresponding bit-true values in a two-component system.

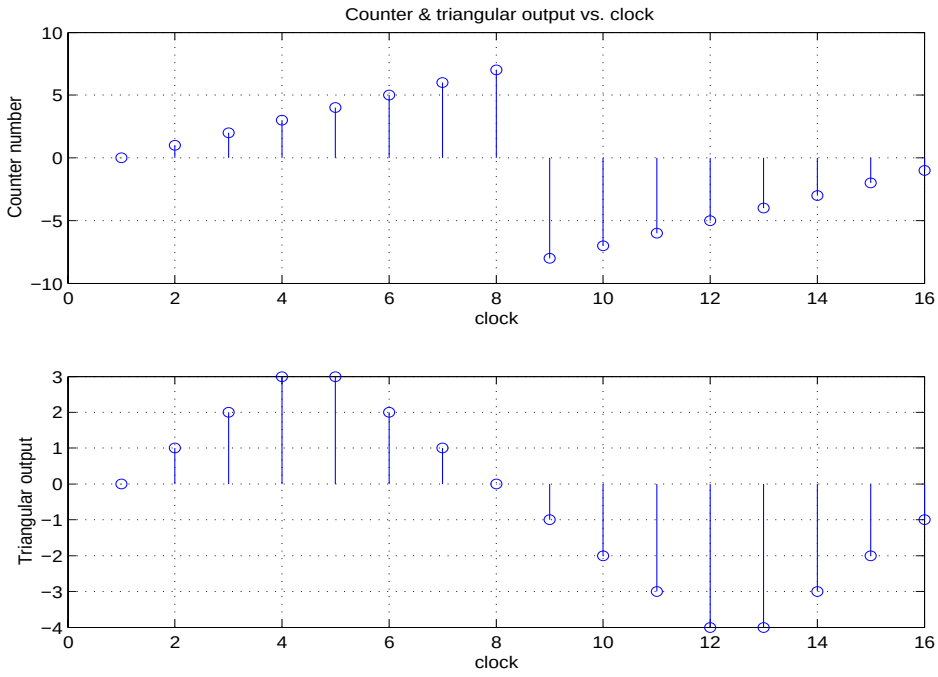

Fig. 5.6: Counter and triangular output with n = 3-bit

The structure of the saturator is shown in Fig. 5.7. This circuit implements the function that sets a limit to the maximum and minimum values of the signal. Whenever these values are exceeded, they are automatically substituted by the saturation values. The register contains the positive saturation level. This is compared to the current input sample and, if the signal exceeds it, the MUX replaces it with the saturation level. Then the signal is compared with the logic negation, which is performed by the in-

verter. If it is smaller, another multiplexer replaces it with the reference value.

Table 5.2: Bit-true values in two-component system

4-bit counter	XOR of 2 MSBs	3-bit triangle
0000	0	111
0001	0	110
0010	0	101
0011	0	100
0100	1	100
0101	1	101
0110	1	110
0111	1	111
1000	1	000
1001	1	001
1010	1	010
1011	1	011
1100	0	011
1101	0	010
1110	0	001
1111	0	000

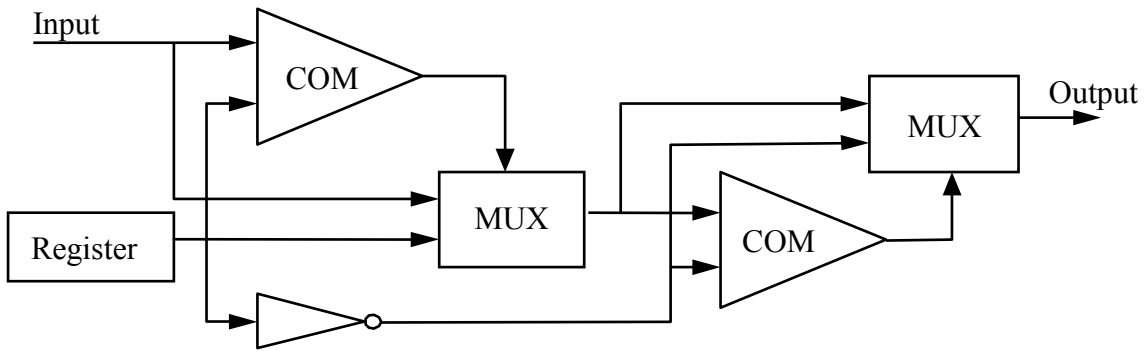

Fig. 5.7: Saturator

5.4.3 Decorrelation of the frequencies

With a classical counter, a trapezoid signal is obtained, containing exactly the same

samples in each period T_0. A direct consequence would be that, after filtering, the samples would still have this periodic distribution. Thus the quantization error on the output samples would not be uniformly distributed in the resolution interval but periodic of the same frequency f_0 of the signal and no longer separable. The noise spectrum is not white but indeed colored. So the hypothesis of non-correlation between signal and error would fall. Consequently, the error power estimations based upon it could not work. Besides, if only a small subset of the possible values is fed to the CUT input over and over, no additional test information will be brought to the CUT. A practical way to avoid this is to set the increment of the counter (this increment is abbreviated as INC in this dissertation). Ideally, to avoid any correlation, the ratio f_0 / f_s (f_0 and f_s mean the desired frequency and the sampling frequency respectively) should be prime. If it can be expressed as the ratio p/q of two mutually prime numbers, then q represents the periodicity of the samples. If q is very large, the error remains indeed periodic but with a period so large that it can be "practically" ignored. The proportion representing the relationship between f_0, f_s, INC and n is:

$$\frac{f_0}{f_s} = \frac{INC}{2^{n+1}} \tag{5.18}$$

But because only integer values for INC are allowed, it may be necessary to adjust the desired frequency slightly until it satisfies:

$$f_0' = f_s \frac{INC}{2^{n+1}} \tag{5.19}$$

Moreover, INC should be rounded towards the next odd integer so that the ratio $INC / 2^{n+1}$ may be irreducible. As an example, consider having to generate a $f_0 = 1\,kHz$ sinusoidal waveform at $f_s = 48\,kHz$:

$$INC = \frac{10^3}{48 \cdot 10^3} 2^{n+1} = \frac{2^{n-3}}{3} \tag{5.20}$$

which, for instance, with an n = 16 bit representation, becomes $INC = 2730.6666\cdots$. Rounding to the nearest odd integer it gives INC = 2731, which also happens to be prime. Then the final frequency in reality is:

$$f_0' = \frac{48 \times 2731}{2^{17}}\,kHz \rightarrow f_0' = 1.00012207031250\,kHz \tag{5.21}$$

which has a relative error of 122 ppm. It can be seen that the frequency error introduced can be made as small as desired by enlarging the word length. For applications where tolerance is smaller, it can be made comparable to the machine clock's jitters.

Since the sampling rate of the CUTs to be introduced in Chapter 7 is 4 MHz, a set of frequencies are illustrated in Table 5.3, which can be obtained from such fixed sampling rate (4 MHz) with different values of *INC* and *n*.

Table 5.3: Frequencies obtained with different *INC* and *n*

n ***INC***	**12**	**13**	**14**	**15**
1	488.28	244.14	122.07	61.03
3	1464.84	732.42	366.21	183.10
5	2441.40	1220.70	610.35	305.17
7	3417.96	1708.98	854.49	427.24
9	4394.53	2197.26	1098.63	549.31
11	5371.09	2685.54	1342.77	671.38
13	6347.65	3173.82	1586.91	793.45

When a two's complement modulo 2^{n+1} counter is used, the saturator of Fig. 6.7 would not be symmetric, as the binary representation is not symmetric either. Instead, if *S* is the chosen saturation level on the positive side, then -(*S*+1) must be chosen for the negative side. Otherwise, the positive values will make up a little less than half-period and the negative values a little more than half-period. As a result, even multiple harmonics will show up in the spectrum. If the suggested levels are employed, the wave remains undistorted and there results only a DC component. If this cannot be tolerated, the best solution is clearly to use a counter with 2^{n+1}-1, i.e. one that wraps at $\pm(2^{n+1}-1)$ generating a symmetrical saw tooth.

5.4.4 Aliasing

Let x_1 be the signal obtained from sampling a continuous trapezoid wave of periodicity $1/f_0$ with $INC = 1$ at a certain sampling rate f_s. The frequencies f_0 and f_s are correlated so that $f_s / f_0 = 2^{n+1} = N$ and x_1 has *N* samples per period: *N* is the periodicity of the discrete signal. Let now x_2 represent the signal obtained by sampling with f_s the

continuous trapezoid wave with increment *INC* = *K* as described in Chapter 5.4.3. For simplicity, K is supposed to be prime with respect to N (it is sufficient that it be odd), so that *N* is still the periodicity of the discrete signal x_2, except that it takes KT_0 (*K* cycles) to cover it.

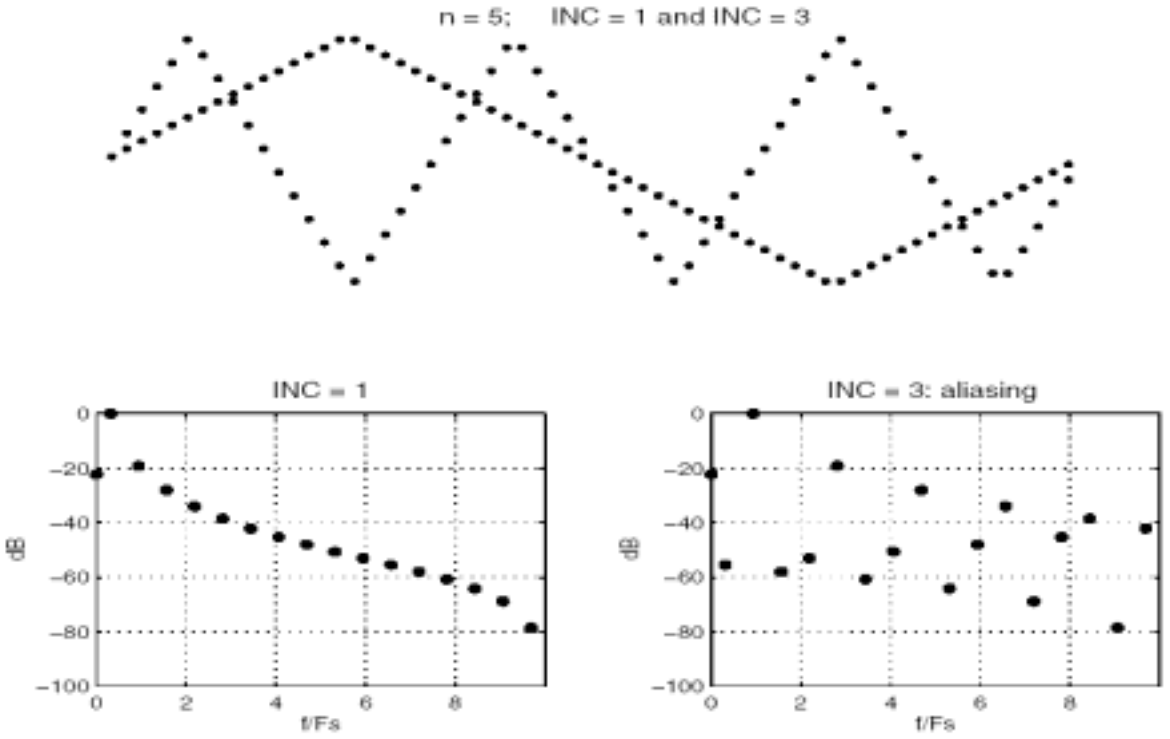

Fig. 5.8: Spectra of discrete triangular waves obtained with $n = 5$, $f_0 = 1$ kHz, $f_s = 20$ kHz and different counter increments

From signal theory and the Discrete Fourier Series [63], it is known that *N* frequency components are sufficient to represent an *N*-periodical signal. Hence, x_1 has in its spectrum the corresponding first (odd) a_{2j+1}, for $j = 0\ldots [N/2]$, whereas x_2's spectrum contains the harmonics a_{2j+1}, for $j = 0 \ldots [N/(2K)]$. Now in both cases the sampling frequency, and hence the band, are the same. But that in the first case the spectrum will be clean whereas in the second it will show aliasing of those odd harmonics falling beyond the normalized frequency 1/*K*. The trick of using a counter step other than unity in practice corresponds to a decimation of the signal. With x_2 as a decimation of x_1, the spectrum of x_2 is that of x_1 dilated *K* times and folded into the band $[-f_s/2, f_s/2]$ which is illustrated in Fig. 5.8.

Unfortunately, “decimating" without reducing the sampling rate is possible only in software generation. In hardware, it should be thought of appropriate sampling rates

and decimation factors that allow realizability. It should be noted that the compulsion to use a higher generation rate reflects into a coarser frequency grid as described in Chapter 5.4.3. Fortunately, in this case – codec chip testing – f_0 is not tightly bounded. Eventually, the signal has to be interpolated to the frequency of the CUT.

5.4.5 The anti-aliasing filter

A signal to be decimated needs to be smoothed by an anti-aliasing filter in order to attenuate the high frequency components which would fall into the band of the decimated signal and thus would degrade the signal [63]. It is common to use a low pass filter for this purpose, but another structure so-called sinc-filter which is easier to realize and adopt for multistage filter banks is widely used for the decimation of a signal as well [85-88]. Essentially, this filter has the following transfer function:

$$H(z) = \left(\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \right)^K \tag{5.22}$$

the corresponding magnitude is shown in Fig. 5.9 and given by the equation (5.23):

$$| H(j\omega) | = \left(\frac{1}{M} \cdot \frac{\sin(\omega M / 2)}{\sin(\omega / 2)} \right)^K \tag{5.23}$$

ω is the normalized frequency in radiant per second: $\omega = 2\pi f / f_s$. Increasing the exponent *K* corresponds to cascading more basis structures. This filter is not a low pass filter, but it serves equally well the purpose. Its *M*/2 spectral zeros

$$f_k = k \frac{F_s}{M} \qquad for \quad k = 1...M/2 \tag{5.24}$$

fall in the centre of the aliased spectra, so it is sufficient that the stop bands be wide enough to contain the replicas:

$$B_k = f_k \pm B \tag{5.25}$$

On the other hand, the pass bands are "don't care" bands, for no signal component falls

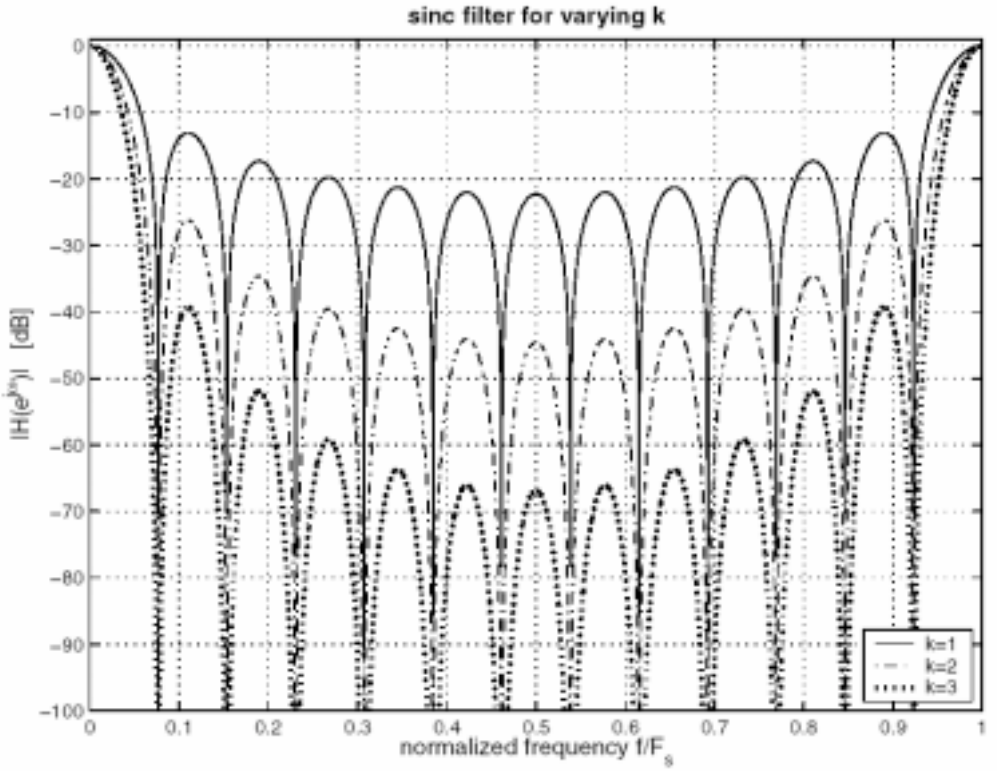

Fig. 5.9: Magnitude of sinc transfer function for varying *k*

in such frequency ranges. A low pass anti-aliasing filter attenuates everything after a certain frequency, whereas a sinc filter attenuates only where necessary. This filter is applicable for decimation purposes only when the stop bands are small compared to the sampling rate and it works well in multistage filter banks. It is very simple to realize in hardware and doesn't even require quantization of the coefficients, since they are all equal to one. It can be realized as a FIR filter based on delay-line and adders as well as a less complex IIR filter. Factoring H(z) in the product of its numerator and denominator and introducing the intermediate sequence $W(z)$:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{Y(z)}{W(z)} \cdot \frac{W(z)}{X(z)} \tag{5.26}$$

the sinc-filter can be thought of as the cascade of an accumulator of equation

$$\frac{W(z)}{X(z)} = \frac{1}{1-z^{-1}} = \sum_{i=0}^{n} x[i] \quad \rightarrow \quad w[n] = w[n-1] + x[n] \tag{5.27}$$

and a differentiator

$$\frac{Y(z)}{W(z)} = 1 - z^{-M} \quad \rightarrow \quad y[n] = w[n] + w[n-M] \tag{5.28}$$

After decimation, the output sequence becomes $y[m] = y[n = mM]$. The operation of decimation reflects itself in the z-domain as a redefinition of the variable: If a pace defined by nT is converted to mTM (what is simply indicated through the normalized discrete time variables n and m), it can be taken into account in the transformed domain by introducing the complex variable $z' = z\,M$ for transforms of signals decimated by a factor M. This leads to a more efficient architecture for the sinc-filter, which is illustrated in Fig. 5.10.

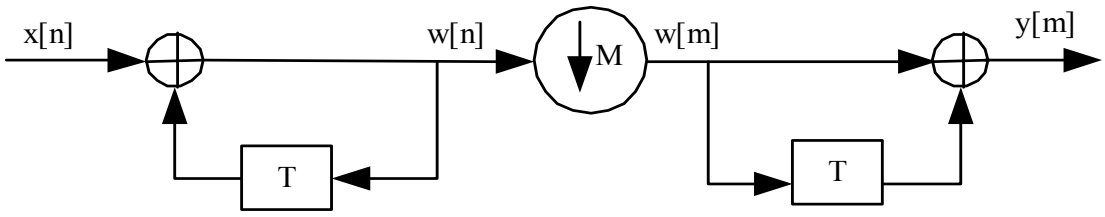

Fig. 5.10: Signal flow graph of sinc-filter

If the decimation takes place just after the accumulator and just before the differentiator, then only a single delay is needed:

$$\frac{Y(z)}{W(z)} = 1 - z^{-1} \tag{5.29}$$

which results in the fact that the computing time is saved. The normalization factor $1/M < 1$ should be taken into account. Quantization over n fractional bits

$$\frac{1}{M} \rightarrow \frac{[2^n / M]}{2^n} \tag{5.30}$$

will not cause the transfer function to be modified, but to be rigidly translated by the quantity

$$\frac{(1/M)_q}{1/M} \rightarrow \frac{M[2^n / M]}{2^n} \tag{5.31}$$

In fact, this is a scaling of the signal and not a coefficient multiplication, which causes eventually the signal not to be full-scale. An alternative to scaling is to append guard bits, which will be explained in the following section.

5.4.6 The low pass filter

In principle, the low pass filter can be placed directly after the sinc-filter. But sometimes the sampling frequency is so huge in comparison with the pass band of the filter that the filter would become a selective filter. And the implementation of a selective filter is a big task for a designer. Therefore, the signal should be decimated to a rate lower than the relatively higher original sampling rate at first, and then a filter with more relaxed requirements is designed. The parameters should be chosen carefully in such a way that the necessary interpolation filters are the same ones used by the chip in functional mode. These interpolation filters bring the low pass filtered signal to the CUT frequency. In this way, the existing hardware is reutilized.

5.4.7 Summary

Fig. 5.11 illustrates the block scheme of this concept in the top level. This method can be summarized as a careful selection of certain parameters in order to satisfy realizability and efficiency of the resources. Then the following quantities can be distinguished:

- f_0: fundamental frequency of the sinusoidal waveform; must belong to voice-band, although not strictly fixed.

- f_{s1}: frequency at which the trapezoid waveform is generated; determines the resolution of frequencies that can be generated.

- *INC*: increment of the counter in the circuit that generates the trapezoid signal; causes a certain amount of aliasing, hence limiting the maximum final SNR of the generated sinusoidal stimulus to that of the band $[0, 5f_0)$; should be odd to guarantee that the error has a maximum periodicity.

- *DEC*: decimation factor; has to bring the signal to a lower frequency $f_{s2} = f_{s1} / DEC$ which allows the realizability of the low pass filter: if it is too high the filter becomes too selective; design calculations have shown that $f_{s2} <$ 64 kHz is proper for a low pass filter with a pass band of 4-6 kHz; the frequency f_{s2} should also be such that the interpolation filters already present on chip can be re-utilized; should be odd to guarantee that the error has a maxi-

mum periodicity.

- *n*: number of bits; fixes signal's dynamic range; maximum error periodicity is 2^{n+1} samples.

- *S*: value at which the trapezoid signal is saturated; allows control of power spectral density distribution.

- *k*: degree of decimation sinc filter; attenuates aliasing frequencies.

These quantities are tied with one another according to the relationships illustrated in the previous sections, in particular by the equation (5.32):

$$f_0 = f_{s2} \frac{INC \cdot DEC}{2^{n+1}} \tag{5.32}$$

It is up to the designer to find the choices that meet the system's requirements. A design example will be given in Chapter 7.

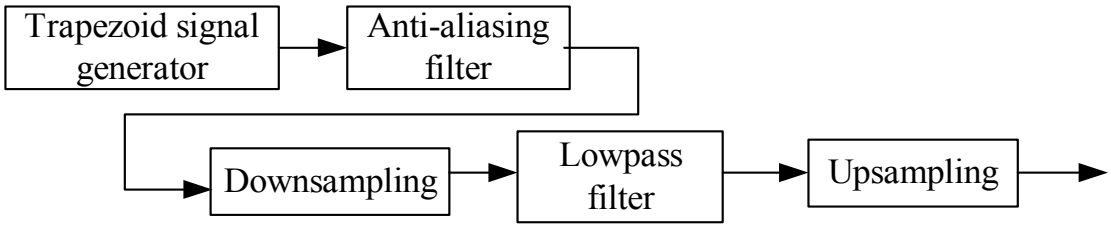

Fig. 5.10: Block scheme for generation concept

5.4.8 Discussion of the concept

When this concept is applied to a real physical system, it is obvious that the signal generated with this concept is in no way with an unlimited resolution. In fact, there are mainly three factors which contribute to the limitation of resolution that the sinusoidal waveform generator can achieve: 1) the algorithm; 2) the quantization error of the coefficients; 3) the round off error

1) The contribution of the algorithm

In this algorithm, an INC not equal unity is employed to avoid the frequency correla-

tion between the signal frequency and the sampling rate. Then, because the INC must be integer, the desired frequency is changed into

$$f_0' = f_s \frac{[INC]}{2^{n+1}} \tag{5.33}$$

which is derived from (5.17). There is $[INC] \in (INC-1, INC]$, which means the maximum error due to the integrity of the INC is one. Therefore, the offset (maximum) of the desired frequency is illustrated by (5.34):

$$\Delta f_0 = f_0 - f_0' = \frac{f_s}{2^{n+1}} \tag{5.34}$$

This means that by a fixed *n*, the bigger the sampling rate f_s, the greater the offset of the desired frequency. Similarly, by fixed f_s, the bigger the *n*, the smaller the offset of the desired frequency. Then the offset can be expressed in a relative form:

$$R(\Delta f_0) = \frac{\Delta f_0'}{f_0} = \frac{f_0 - f_0'}{f_0} = \frac{K}{2^{n+1}} \tag{5.35}$$

where *K* is the sampling ratio and is equal to f_s / f_0. The algorithm needs *INC* times of the period to cover the whole testing process, namely the whole generation time is INC / f_0. From the above discussion, the following conclusions can be drawn:

- When f_s, f_0 and *n* are fixed, the *INC* can be derived from these parameters and the whole generation time is obtained. Moreover, the offset of f_0 can be further derived and exam whether it lies in the acceptable ranges.

- When f_s, f_0 and Δf_0 are fixed, the bit number of the system, so-called *n*, can be derived, which dominates the overhead on chip. If $R(f_0)$ is equal to 10^{-6} (For applications where the tolerance is smaller, it can be compared to the machine's clock jitter), the relationship between the *n* and *K* (sampling ratio) is illustrated in Fig 5.12.

- When f_0 and f_s are fixed, the n must be enlarged (bigger overhead) in order to get a smaller frequency offset. Meanwhile the INC should be enlarged, too, in order that the f_0 will keep the same value.

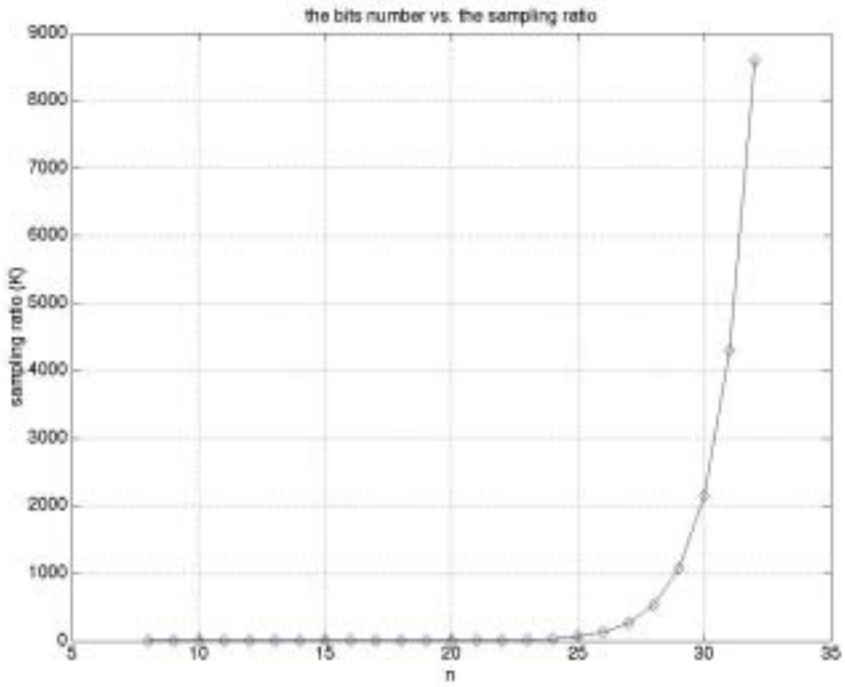

Fig. 5.12: The different sampling ratio due to the bit number

- In fact, the introduction of the INC can give another benefit: if both f_0 and n are fixed, which means the quantization level is fixed, the INC can adjust the sampling rate (f_s) to a proper value which is acceptable for the design. As an example, considering a digital system whose highest clock is limited to 1 MHz, if a signal with 1 kHz frequency and 16 bits resolution is wanted, the sampling rate would be 131 MHz with INC = 1 (of course there is frequency correlation due to INC = 1); However, if an INC = 2731 is employed, the sampling rate would be changed into 48 kHz, which can finally meet the system requirements.

- Moreover, this algorithm can only generate a signal whose frequency lies in some fixed frequency, which is determined by the equation (5.18). Some examples with f_s = 4 MHz are already available in Table 5.3.

2) The quantization effects of the system

Due to the finite word length for a real digital system, the quantization effects are very important issues from concept to implementation for a designer. There are two types of

quantization of a digital system: coefficient quantization and round off quantization. Both of them will be discussed in the next content.

a) Coefficient quantization

For this concept, only the coefficient quantization in the low pass filter needs to be considered. The coefficients in other components are either a finite sum of powers of 2 (trapezoid signal generator) or positive/negative one (the anti-aliasing filter). Therefore they are not needed to be quantized. If the coefficients of the low pass filter are expressed approximately as finite sum of powers of 2, this inevitably results in a change of the positions of the roles and the zeros. Thus this change affects the real cutoff frequency and the stability further. Because the low pass filter has a very relax transient band – typically from 3^{rd} harmonic distortion to 5^{th} harmonic distortion of the signal frequency, the cutoff frequency is almost unaffected by coefficients quantization. As for the stability, according to the theory of bounded-input, bounded-output (BIBO) stability [66], the system is stable, only when the poles indeed do not move out of the unit circle but remain inside the unit circle, so that the amplitude of the signal never increases over time.

b) Propagation of round off error

As it is known, not only coefficient quantization but also the necessary re-quantization after a multiplier, due to the finite register length, introduces noise in a system. Such re-quantization is referred to as round off noise. If two binary fractions are multiplied, the result will need a number of binary digits equal to the sum of the digits of the factors. Maintaining this precision in an IIR filter would mean increasing the number of digits for the number representation at each recursion, which results in endless word length. That is practically unacceptable.

We distinguish between internal representation (characterizing the precision, with which the calculations are performed) and output representation (the representation of the samples exiting the system). The latter is determined by the adjacent external components of the front-end, in particular the number of bits of the CUT. The former is chosen as a tradeoff between the degree of precision desired and the acceptable expenditure.

Typically, the internal register length is that of the input (output) extended on the Most

Significant Bit (MSB) side by so-called guard bits to protect the filter from overflow and on the Least Significant Bits (LSB) side by so-called rear bits to keep the power of the round off error under control. The role of rear bits in error propagation will be examined. The error introduced into the system is essentially the error denoted by $e_{roundoff}$, due to the multiplier or adder as shown in Fig. 5.13. This error is non-linear in nature, but the calculations are considerably simplified if some assumptions are made. The goal of such assumption is to allow this error to be considered as an additive, hence preserving linearity and superposition. If the general error is denoted by *e* and the general signal by *x* at a certain node, the following assumptions are made [63]:

1. The *e* is a statistical variable uniformly distributed in its interval of definition.
2. The *e* and the signal *x* are uncorrelated.
3. All errors have white spectra and are uncorrelated with one another.

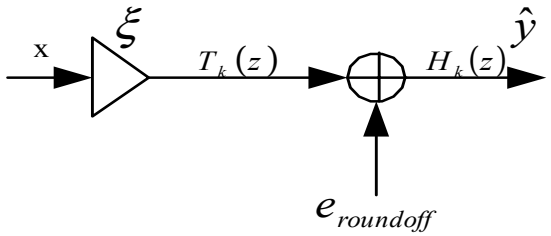

Fig. 5.13: model of round off error

These hypotheses are obviously not correct because *e* is indeed a function of x:

$$e = e(x) = x_{quant} - x \tag{5.36}$$

where x_{quant} is referred as the quantized signal. But these hypotheses are acceptable in the most cases.

Round off error that is $e_{roundoff}$ in Fig. 5.13 depends on the multiplier or adder, which means that the inner word-length is assigned to the partial results on the multiplication algorithm or addition algorithm. The intention is obviously to keep round off noise as low as possible. Design specifications usually fix the input word length, the output word length and the desired SNR. This leaves some margin for the internal word length to minimize the consequences of truncation. To reduce the magnitude of overflow and rounding errors, the word width must be sufficiently wide.

The computation of digital filter algorithms usually requires many multiplications. A good way of minimizing chip area is to substitute multipliers with equivalent shift-and-add operations, a choice of which is WDF which was introduced in Chapter 4. This type of filter has the characteristic that it reacts with little sensitivity to the coefficients. This is very important in the application, where multipliers are replaced by shifters and adders. Shortening of the coefficients can save calculation time and round off noise is reduced because fewer bits are truncated. To determine the internal word length, two types of countermeasures can be taken, according to two transfer functions:

1. The gain from the input to the node $T_k(Z)$.
2. The gain from the node to the output $H_k(Z)$

From point (1), the guard bits are determined so that overflow does not occur, or the scaling factor is determined to reduce the amplitude of the input signal:

$$\begin{aligned} w_k[n] &= \sum_{m=0}^{\infty} t_k[m]x[n-m] \\ |w_k[n]| &\le x_{\max}\left|\sum_{m=0}^{\infty} t_k[m]x[n-m]\right| \end{aligned} \tag{5.37}$$

Assume that each fixed-point number represents a fraction, each node in the network must be constrained to have a magnitude less than 1 ($|w_k| < 1$). Then a sufficient condition to avoid overflow is:

$$x_{\max} \cdot \underbrace{\left|\sum_{m=0}^{\infty} t_k[m]x[n-m]\right|}_{L_1} < 1 \tag{5.38}$$

The sum of the series is the L_1-norm of t_k. This can be achieved either by scaling x to reduce $x_{\max}$ or by appending guard bits. The L_1 scaling assures that overflow never happens. Another approach is to assume the input to be a generic tone. Overflow is avoided for all sinusoidal signals if

$$x_{\max} \cdot \max\underbrace{\left|T_k\left(e^{j\omega}\right)\right|}_{L_\infty} < 1 \tag{5.39}$$

From point (2), the rear bits are determined in the following way. For linear systems as shown in Fig. 5.13 the output signal is given by the convolution of the input signal and

the pulse response. If e_k is the round off error injected at the k th node, h_k the relative impulse response and y_k the output due only to e_k (the principle of superposition deriving from linearity allows to switch off all other inputs and error sources), then:

$$y_k[n] = \sum_{m=0}^{\infty} h_k[m]\, e_k[n-m] \tag{5.40}$$

The actual output $\hat{y}$ of the system will be a sum of the expected output y and the propagation of the round off errors to the output:

$$\hat{y} = y + \sum_k y_k \tag{5.41}$$

Assuming the injected noise is non-correlated with the clean output y; their powers P_{yk} may sum up and add to the global noise term. The generic contribution P_{yk} can be decreased by increasing the system's precision, for example by adding rear bits.

5.4.9 Limitation of the linearity of the concept

In theory, a sinusoidal waveform with an arbitrary resolution can be generated using this concept, which means that the SNR of the signal is unlimited. But in application, it is impossible to achieve such a high resolution mainly due to the following three factors: 1) the non-ideality of the transient band of the low pass filter. The goal of the low pass filter is to remove the higher harmonics so that only the fundamental frequency is available at the output. The narrower the transition bands of the filter, the better its performance. But in a real physical system, the transition band can not be unlimitedly narrow. So the non-ideality of the transient filter affects the overall performance of this concept; 2) the quantization of the coefficients applied in the concept. The quantization of the coefficients changes its original value and influences the SNR of the output signal directly or indirectly; 3) the introduction of *INC*. From the discussion in the section above, it is known that the trick of using a counter step of *INC* other than unity in practice corresponds to a decimation of the signal. Therefore it will show aliasing of those odd harmonics falling beyond the normalized frequency 1/*INC*. If the sampling rate is denoted by f_s, the signal with *INC* = 1 by x_1 and the signal with *INC* other than unity by x_2, then the spectrum of x_2 is that of x_1 dilated *INC* times and folded into the band

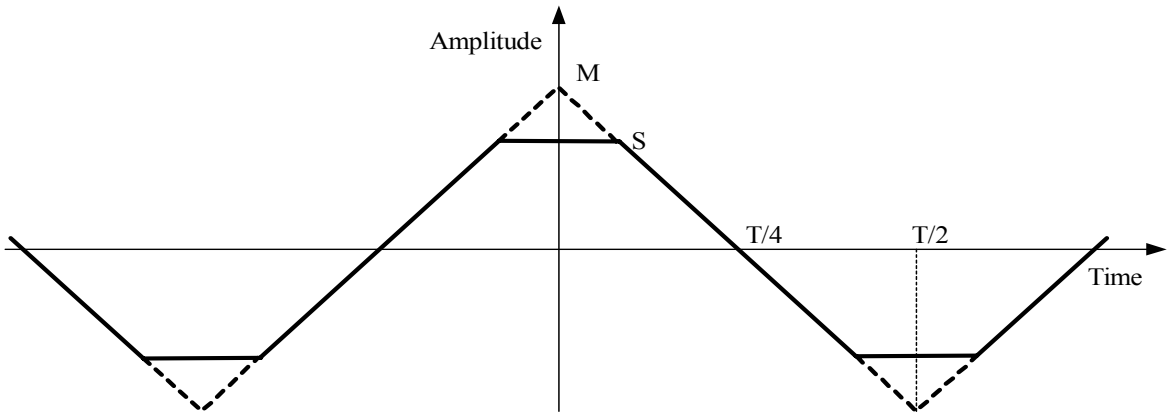

Fig. 5.14: Trapezoid waveform

$[-f_s/2, f_s/2]$, which is illustrated in Fig. 5.10. This means that an *INC* not equal to unity can introduce some harmonics falling below the cut-off frequency of the low pass filter, which would decrease the SNR of the signal at the output. The effects of these three factors on the SNR will be discussed as follows.

Firstly, the situation with *INC* = 1 will be considered, which means that there is no in-band distortion due to decimation. Then the effects of the *INC* not equal to unity will be discussed. The coefficients of the Fourier transform of a trapezoid waveform like in Fig 5.14, with a period of *T*, a saturation level of *S* and *M* being the amplitude of a triangular waveform with the same frequency, can be obtained:

$$(a_k) = \frac{2M}{k^2\pi^2}\left[1-(-1)^k\right]\cos\left(\frac{k\pi}{2}\left(1-\frac{S}{M}\right)\right) \Rightarrow |a_k|_{odd} = \frac{4M}{k^2\pi^2}\left|\sin\left(\frac{k\pi}{2}\frac{S}{M}\right)\right| \quad (5.42)$$

Thus

$$\begin{aligned} |a_1| &= \frac{4M}{\pi^2}\left|\sin\left(\frac{\pi}{2}\frac{S}{M}\right)\right| \\ |a_3| &= \frac{4M}{9\pi^2}\left|\sin\left(\frac{3\pi}{2}\frac{S}{M}\right)\right| \\ &\cdots\cdots \end{aligned} \quad (5.43)$$

In the ideal situation, the low pass filter should filter out all the harmonics except the fundamental frequency, which means that the achievable SNR would be infinite. Unfortunately, this assumption is no longer suitable in a real system, because the transient band of a low pass filter that can be implemented extends from the frequency range of 3rd harmonic distortion to the frequency range of 5th harmonic distortion and its cut-off

frequency lies in the the frequency range of 5th harmonic distortion due to design issues. Therefore, the achievable SNR will never be infinite.

Now let's suppose the low pass filter attenuates the 3rd harmonic distortion by *D* dB and blocks all the other harmonic distortions. Then according to Parseval's theorem, the SNR of the output signal will be:

$$SNR_{output}\,[dB] = 10\log\frac{|a_1|^2}{|a_3|^2 \cdot 10^{-\frac{D}{10}}} \tag{5.44}$$

The SNR of the output signal is:

$$SNR_{output}\,[dB] = 19.085 + 20\log\left|\sin\left(\frac{\pi S}{2M}\right)\right| - 20\log\left|\sin\left(\frac{3\pi S}{2M}\right)\right| + D \tag{5.45}$$

Then suppose that S' is the quantized value of S:

$$S' = \frac{[S \cdot 2^n]}{2^n} \tag{5.46}$$

$[S \cdot 2^n]$ means the biggest integer which does not exceed the value of $S \cdot 2^n$. Obviously, the value of $[S \cdot 2^n]$ lies in the range of $(S \cdot 2^n - 1, S \cdot 2^n]$. That is to say, the value of S' lies in the range of $(S - 1/2^n, S]$.

Thus the equation of the SNR can be adjusted to:

$$SNR_{output}\,[dB] = 19.085 + 20\log\left|\sin\left(\frac{\pi S'}{2M}\right)\right| - 20\log\left|\sin\left(\frac{3\pi S'}{2M}\right)\right| + D \tag{5.47}$$

It has been discussed that, if $S = 2M/3$, the 3rd harmonic distortion would be the smallest. If S converges to $2M/3$, then $3\pi S'/(2M)$ will converge to π and $\sin(3\pi S'/(2M))$ will converge to 0.

As it known, the function *sin*(*x*) is a monotonous descending function in a very small range of $(\pi - \Delta, \pi)$ (with $\Delta \rightarrow +0$). Then *sin*(*x*) reaches its maximum value in the point $(\pi - \Delta)$. On the other hand, *sin*(*x*) reaches its minimum value in the point $\pi/3$ in the

very small range of $(\pi/3-\Delta,\pi/3)$. If n is big enough, $1/2^n$ will be comparable with Δ:

$$SNR_{output}[dB] = 19.085 + 20\log\frac{\sqrt{3}}{2} - 20\log\left|\sin\left(\frac{3\pi(\frac{2}{3}M-\frac{1}{2^n}}{2M}\right)\right| + D$$
$$= 17.836 - 20\log\left(\sin\left(\frac{3\pi}{2^{n+1}M}\right)\right) + D \tag{5.48}$$

As an example, with n = 14 bits, M = 1.85 V and the low pass filter attenuating the signal inside the transition band by 50 dB, the maximum achievable SNR is 145 dB, which corresponds to a resolution of 24 bit. Now let us consider the effects of *INC* in the case of that it is not equal to unity. Because the frequency folds itself due to decimation, some higher-order harmonics are re-sampled and would lie inside the signal band. Supposed there are 2^{n+1} points after the FFT and the increment of the counter is *INC*, then the total points are grouped in *INC* sections and there are $2^{n+1}/INC$ points in each section. Thus, the frequencies which leak into the signal band can be expressed as $(K\cdot 2^{n+1}/INC-1)$, by which there is $1 < K < INC$. Here only K = 2 and K = 3 would be taken into consideration, because, with higher K, the amplitude of the distortions become so small that they can be ignored. The harmonics at the frequencies $k_1 = 2^{n+2}/INC-1$ and $k_2 = 3\cdot 2^{n+1}/INC-1$ must be taken into consideration for computing the SNR. Then the final result is:

$$SNR_{output} = 10\log\frac{|a_1|^2}{\left(|a_3|^2+|a_{k1}|^2+|a_{k2}|^2\right)\cdot 10^{-\frac{D}{10}}} \tag{5.49}$$

The output SNR is dependent of many factors. Fig. 5.15 shows the relationship of the bit number and the maximum obtained SNR. In this figure, M is set to 1 and S to 2/3, D is 50 dB and the increment of the counter – *INC* – is fixed to 11, 31, 65 and 77 respectively. Furthermore, f_0 is fixed to 1 kHz which means f_s must be varied according to the change of bit number n, so that equation (5.17) can always be held. From Fig. 5.15, it can be seen that the SNR would not increase any more when n is bigger than 28 bits. Then *INC* is fixed to 65 and f_0 to 1 kHz, 10 kHz, 100 kHz and 1 MHz respectively. The simulation results are shown in Fig. 5.16, from which a similar conclusion can be drawn. So it is reasonable to state that there is no need to design a system, whose word length is more than 28 bits. A much clearer visualization is given in Fig. 5.17 where bits number varies from 4 to 14. From this figure it is obvious that for a

system with enough SNR, the number of bits should not be less than 10 bits. By setting *D* to 35 dB, which means that the low pass filter provides an attenuation of 35 dB in the transition band, Fig. 5.18 can be obtained, where the maximum achievable SNR is smaller than that in the case of 50 dB attenuation. In fact, another conclusion can be drawn: if the sampling rate can be selected freely, the system can reach an identical SNR even if the desired frequencies f_0 are different. This conclusion is very useful if a multi-tone stimulus is needed by a BIST application. Such stimulus is applicable, if the achievable SNR value for the highest frequency component of interest can meet the design requirements.

From above, it can be derived that f_0 and f_s are important factors which contribute to the finally achievable SNR. Therefore, the simulation to show the relationship between the ratio of f_0 and f_s (or, in other words, the normalized f_0) and the maximum achievable SNR is very important. Since the SNR depends on the bit number, the simulations are carried out with different numbers of bit. The results are illustrated in Fig. 5.19. It shows that the SNR becomes worse and its swing is less with a bigger f_0. If f_0 is less than $0.002 f_s$, both the achievable SNR and the swing are acceptable.

Next simulation is intended to examine how the SNR varies when the bit number increases. Last simulation shows that the maximum SNR depends on the ratio between f_0 and f_s, the so-called sampling ratio. Nevertheless, a better SNR is only achievable when the sampling ratio is greater than 1/0.002 = 500. So the simulations are carried out with different sampling ratios (500, 1000 and 2000). In order to illustrate that the system performance would become worse with a sampling ratio smaller than 500, a simulation with a sampling ratio of 200 is performed in addition. The simulation results are shown in Fig. 5.20, from which the conclusion can be drawn that the SNR will increase with an increasing number of bits. The higher the sampling ratio is, the clearer this phenomenon becomes. Let us consider the line (f_0/f_s = 0.005) at the bottom of the figure. The SNR increases no longer even if the number of bits increases, because the sampling ratio is smaller than 500. This coincides with the simulation results in Fig. 5.19 once again.

Now let us have a look at the relationship between SNR and *INC*. Firstly, the increment of the counter is swept from 7 to 113. The results are shown in Fig. 5.21. It seems that the smaller the *INC*, the better the SNR and the smaller the swing. This can easily be explained: when *INC* is small, less harmonics are folded into the pass-band. Thus, a better SNR can be achieved. Then the simulations with different bit number are carried out. Their results are also shown in Fig. 5.21.

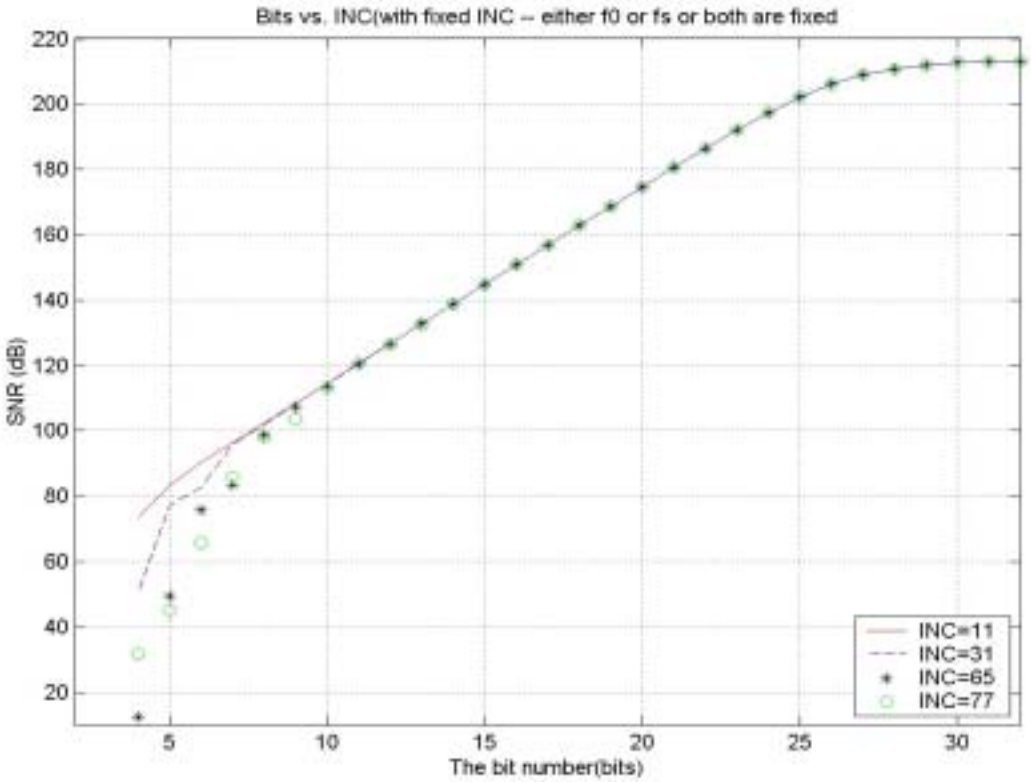

Fig. 5.15: SNR vs. number of bits

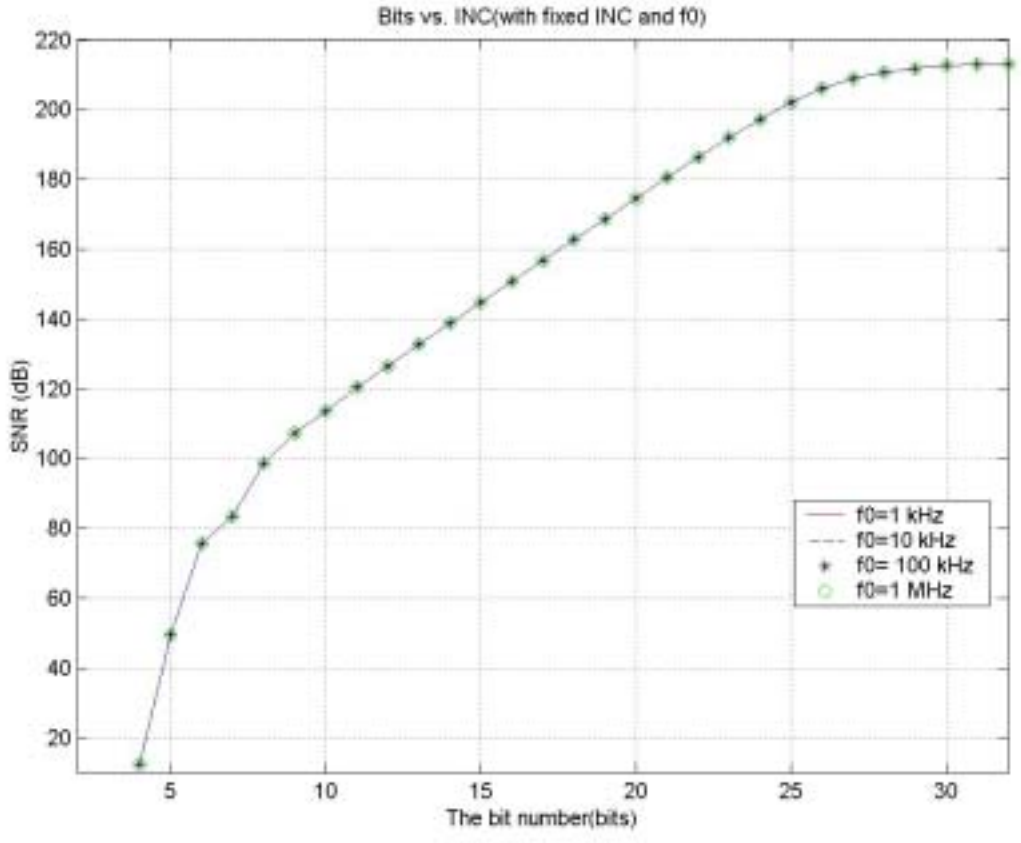

Fig. 5.16: SNR with different f_0

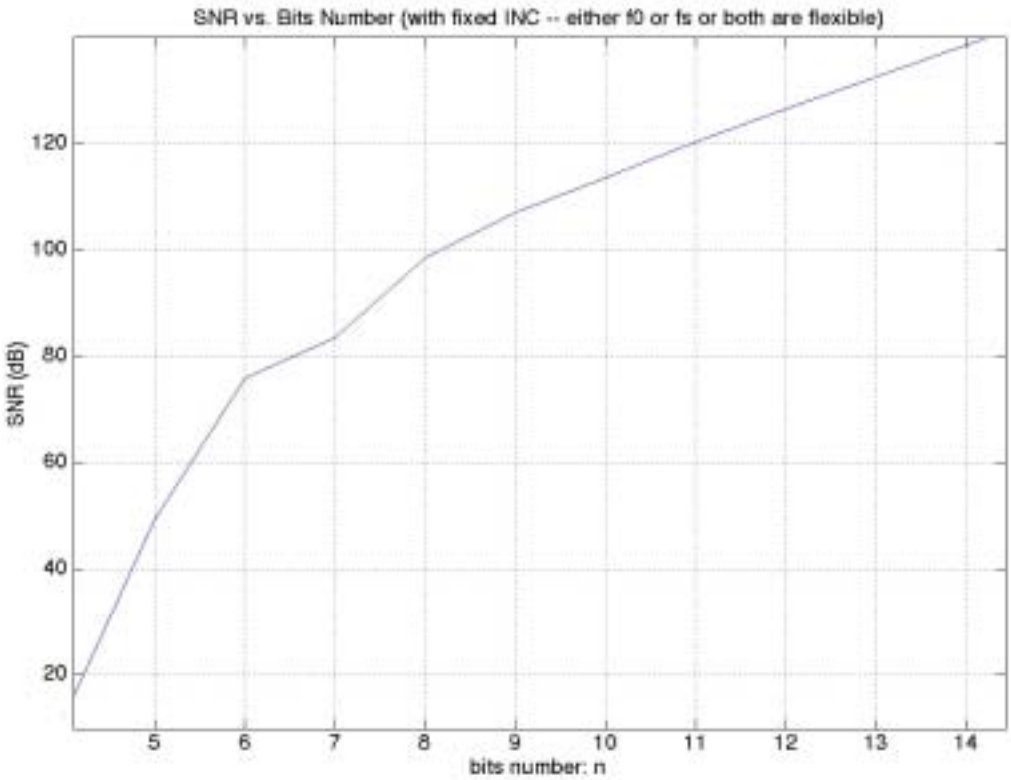

Fig. 5.17: SNR vs. number of bits(*INC* = 65)

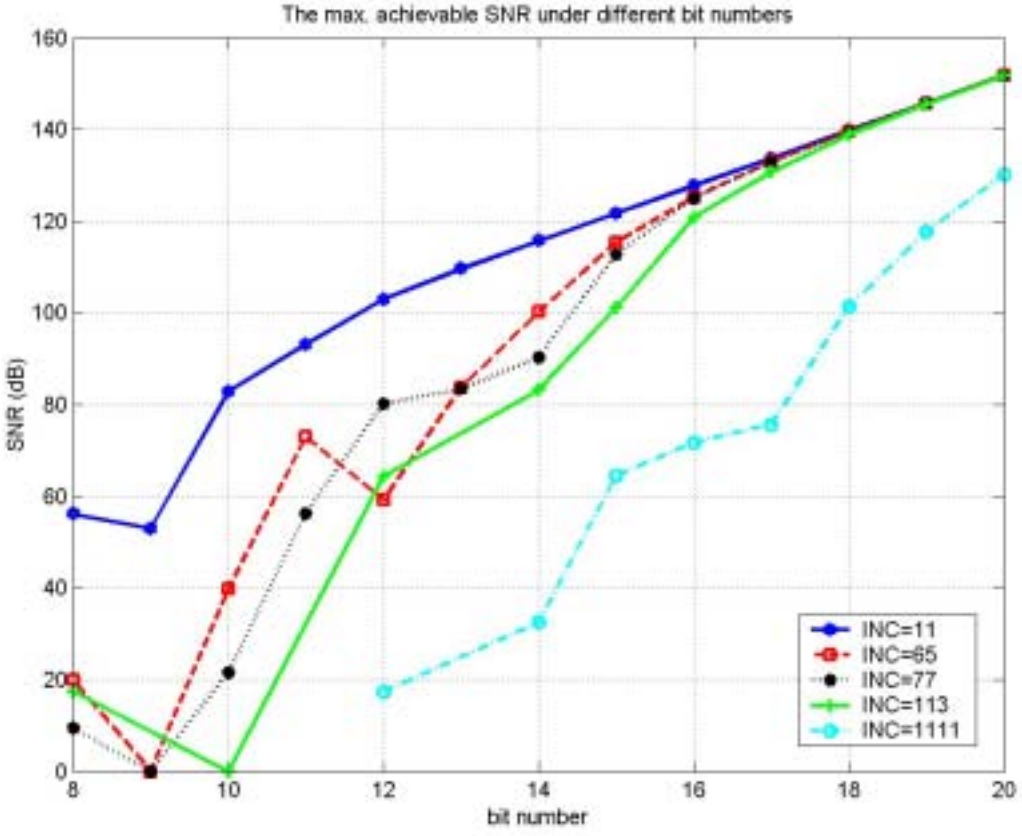

Fig. 5.18: SNR with different *INC*

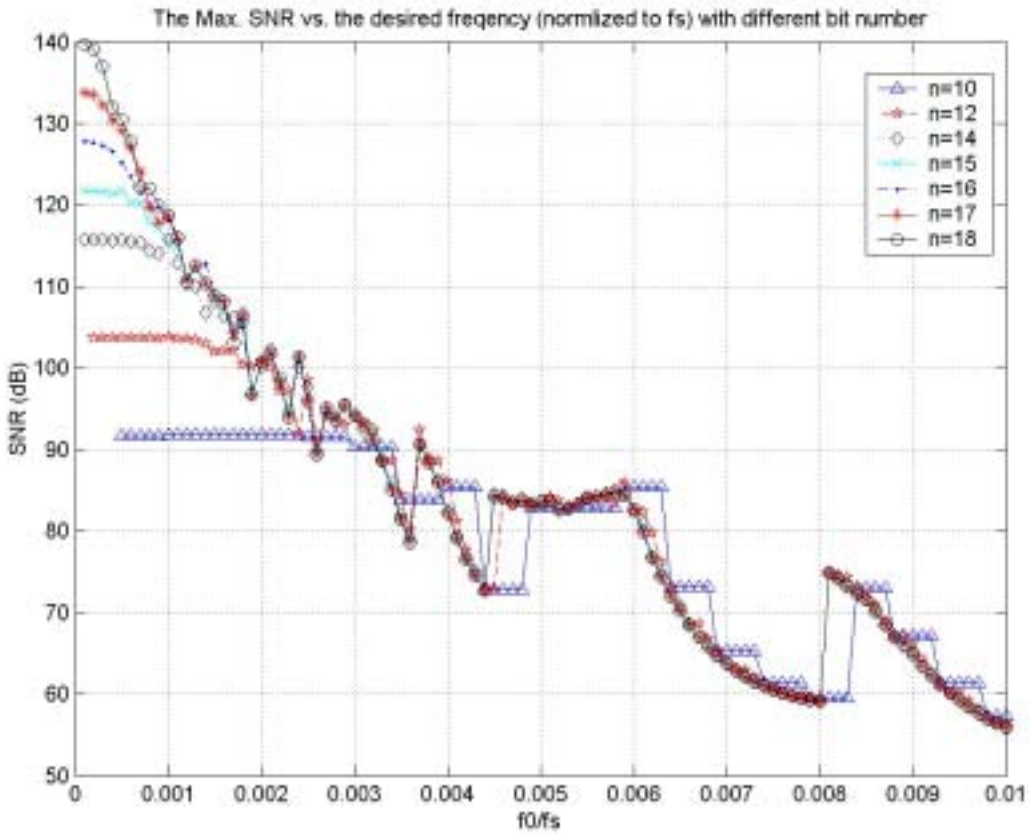

Fig. 5.19: SNR with different number of bits

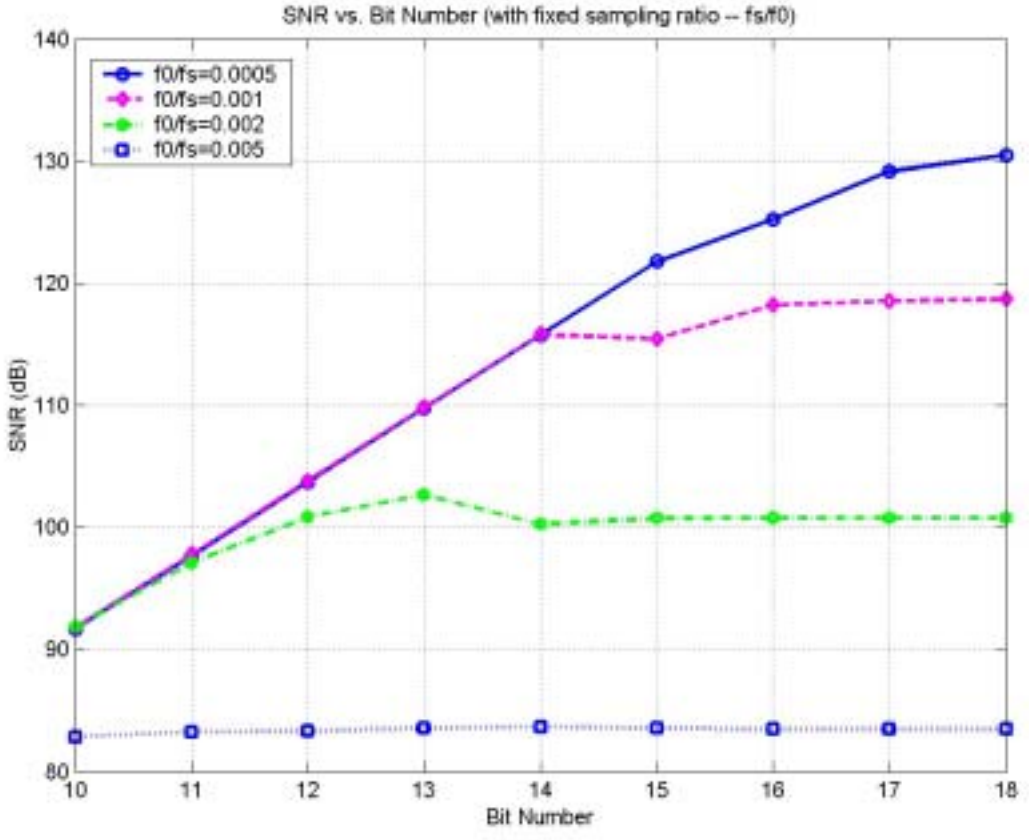

Fig. 5.20: SNR with different sampling ratio

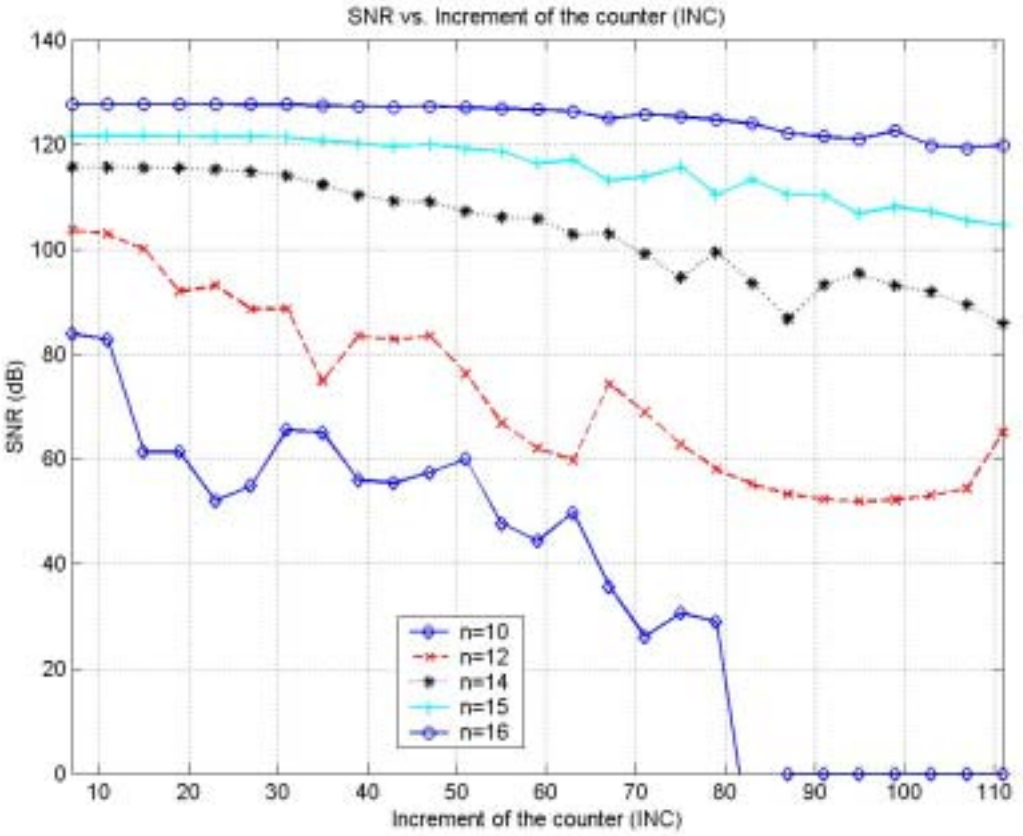

Fig. 5.21: SNR vs. *INC*

In summary, by design and implementation the sampling ratio should be greater than 500 in order to obtain a better SNR (Fig. 5.19). A proper f_s can be determined with a given f_0; a proper number of bits *n* (Fig. 5.20) has to be chosen, from which the derivation of the *INC* (the increment of the counter) can be derived. At last, the whole design can be examined by Fig. 5.21.

5.5 Generation of an analog stimulus on chip

The generation methods introduced above are commonly employed to generate a digital sinusoidal waveform on chip. They can also generate an analog testing stimulus, if they are connected to a DAC. However, there are several problems with such combination. Firstly, the DAC must have a higher speed and a higher resolution than the analog circuitry under test (e.g. ADC), which is not always the case. Secondly, if the DAC is fabricated on chip, it needs the interface circuitry to the DSP on chip which leads to additional overhead on chip. Thirdly, the DAC needs to be verified before the BIST process. But testing a DAC with complex characteristics is a hard and huge task.

An alternative method is to use the over-sampling and noise shaping techniques, so-called Delta-Sigma Modulation (DSM). To combine with some simple additional digital circuitry on chip, a delta-sigma modulator can produce an analog testing stimulus with a very high resolution [39] [40] [61] [71], which can be effectively applied to the BIST scheme for the integrated circuits. The principle of this method is that a ΔΣ (Delta-Sigma) modulator encodes a multi-bit digital input signal into a single bit stream with a peak-to-peak amplitude of Δ using digital signal processing and over-sampling techniques[39] [40]. Fig. 5.22 shows this process. A sinusoidal digital input signal of amplitude A and frequency f_t is oversampled by a sampling rate f_s with $f_s >> f_t$. Then the one-bit stream toggles between the high and low state in such a way that the input signal is encoded into the density of the output waveform. This is called a Pulse-Density Modulated (PDM) signal.

After digitally filtering the one-bit output, the multi-bit digital input signal can be recovered, because the ΔΣ modulation process ensures that the input signal and the quantization error occupy different frequency regions. Similarly, the serial stream can be filtered using an analog filter with bandwidth f_B which is greater than f_t to transform the digital input signal into analog form. But the quantization error lying in-band can not be separated by filtering and remains in the output of the analog filter, which means that the output is not an ideal sinusoidal signal. Its characteristics depend on the over-sampling ratio $f_s / 2f_B$ and the order of the ΔΣ modulator. In the next section a brief introduction to these modulators is provided.

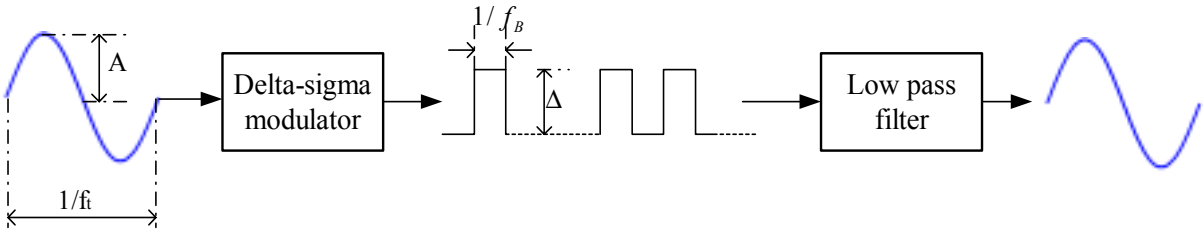

Fig. 5.22: Delta-sigma-based digital encoding of a sinusoid signal

5.5.1 Oversampling technique and ΔΣ modulation

5.5.1.1 Oversampling without noise shaping

Quantization introduces distortion. By assuming that the error e has statistical properties and is independent of the signal, the means square value of the quantization error

e is given by equation (5.50) [72]. This quantization error has equal probability of lying anywhere in the range ± Δ/2, where Δ is the quantization level spacing.

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{5.50}$$

Oversampling occurs when the signals of interest are band limited to f_B while the sampling rate is at f_s , where f_s >2 f_B. The Oversampling Ratio (*OSR*) is defined as

$$OSR = f_s / (2\, f_B) \tag{5.51}$$

Assuming that the quantization noise is white, and noting that the total noise power is e_{rms}^2 in the range of $\pm f_s / 2$, the spectral density of the quantization noise is

$$E(f) = e_{rms}\sqrt{\frac{1}{f_s}} = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \tag{5.52}$$

As shown in Fig. 5.23, after quantization $x_1(n)$ is filtered by *H*(*f*) to create the signal $x_2(n)$, since the signals of interest are all below f_B.

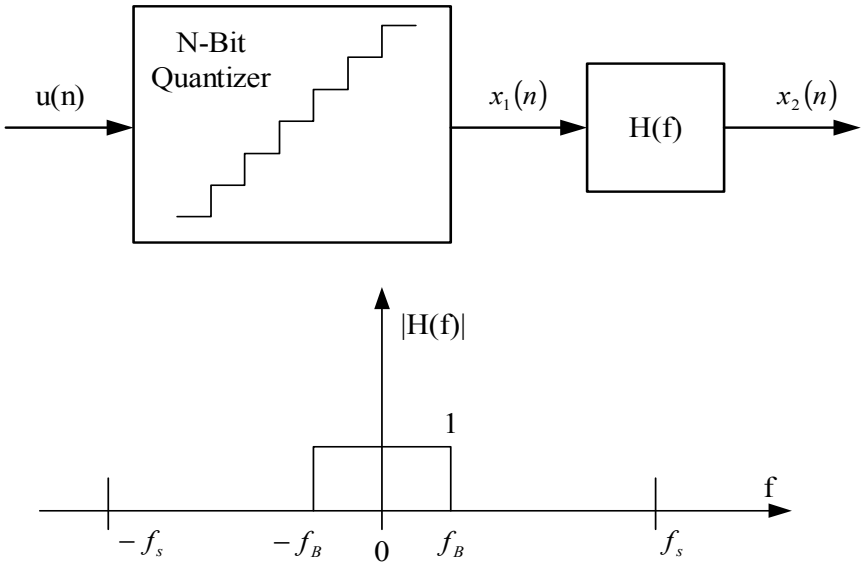

Fig. 5.23: An over-sampling system without noise shaping

This filter eliminates quantization noise (together with any other signals) greater than f_B. Then the noise power P_n that falls into the signal band will be given by:

$$P_n = \int_{-f_B}^{f_B} E^2(f)df = e_{rms}^2(2f_BT) = \frac{e_{rms}^2}{OSR} = \frac{\Delta^2}{12}\cdot\frac{1}{OSR} \tag{5.53}$$

Because the testing stimulus in industry testing is often a sinusoidal signal which is also the testing signal in this dissertation, it is important to examine the SNR performance under the condition of a sinusoidal input.

Assume that the sinusoidal input is quantized by *N*-bits and that its maximum peak value without clipping is $2^N(\Delta/2)$. Then the maximum signal power P_s is given by:

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8} \tag{5.54}$$

The signal power will not change after oversampling and low pass filtering with H(f) due to the assumption that the signal's frequency content lies below f_B. Then the maximum SNR (in dB), which is the ratio of the maximum sinus power to the quantization noise can be calculated:

$$\begin{aligned} SNR_{\max}[dB] &= 10\log(P_s/P_n) = 10\log\left(3\cdot 2^{2N-1}\right) + 10\log(OSR) \\ &= 6.02N + 1.76 + 10\log(OSR) \end{aligned} \tag{5.55}$$

This shows that each doubling of the sampling rate will decrease the in-band noise by 3 dB, increasing the resolution by half a bit.

5.5.1.2 Oversampling with noise shaping

A general noise-shaped delta-sigma (ΔΣ) modulator is shown in Fig. 5.24 [72]. This structure is known as an interpolative structure. The signal transfer function *STF*(*z*) and the noise transfer function *NTF*(*z*) of this modulator are:

$$\begin{cases} STF(z) = Y(z)/U(z) = H(z)/(1+H(z)) \\ NTF(z) = Y(z)/E(z) = 1/(1+H(z)) \end{cases} \tag{5.56}$$

The zeros of the noise transfer function will be equal to the poles of *H*(*z*). When *H*(*z*) approaches infinity, *NTF*(*z*) will reach zero. If we choose *H*(*z*) in such a way that its

magnitude is large over the frequency band of interest, we can noise-shape the quantization noise in a useful manner. With such a choice, the signal transfer function will approximate unity over the frequency band of interest [72]. Moreover, the noise transfer function *NTF*(*z*) will approximate zero over the same band. Thus the quantization noise is reduced over the frequency band of interest while the signal itself is unaffected.

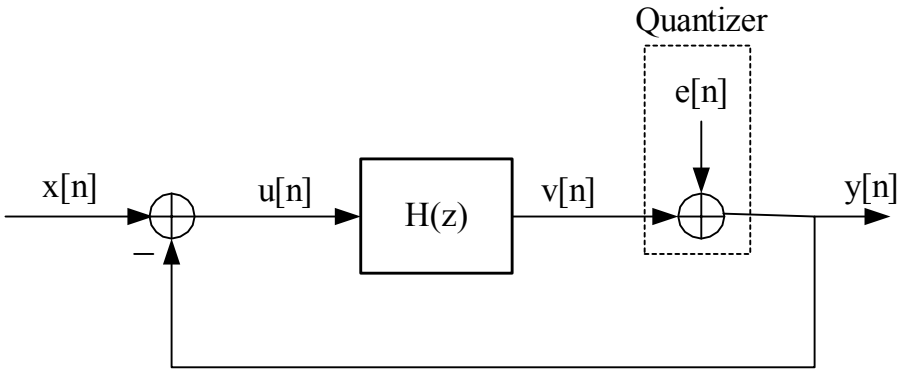

Fig. 5.24: The linear model of the modulator

5.5.1.3 First order delta-sigma modulator

The structure of the first-order ΔΣ modulator is shown in Fig. 5.25. The modulator consists of an integrator, an internal ADC or quantizer, and a DAC used in the feedback path. It can easily be shown that the output of the integrator is

$$V[i] = x[i-1] - e[i-1] \tag{5.57}$$

and the quantized sign is

$$V[i] = x[i-1] - (e[i] - e[i-1]) \tag{5.58}$$

The DAC in the modulator is required to be nearly as linear as the overall conversion resolution. Any DAC nonlinearity can be modeled as an error source that adds directly to the input. This error source benefits from the oversampling but unlike $e[n]$, which models the ADC quantization error, is not subject to the noise shaping. 1-bit DACs are frequently used in oversampling techniques. The advantage of a 1-bit DAC is that it is inherently linear [72]. It has only two output values, and since two points define a straight line, no trimming or calibration is required. This inherent linearity is one of the major motivations for making use of oversampling techniques with 1-bit converters. It

is common to use a 1-bit DAC and a corresponding 1-bit quantizer, which is simply a comparator. Consequently, if the sampling frequency is high enough, the sigma-delta ADC allows the use of a 1-bit quantizer to achieve high overall resolution.

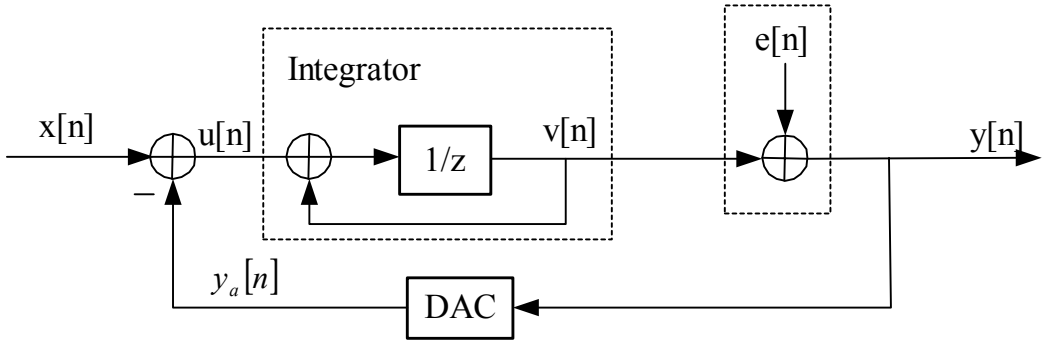

Fig. 5.25: First order delta-sigma modulator

To calculate the effective resolution of the ΔΣ (Delta-Sigma) modulator, we assume that the error e behaves like white noise that is uncorrelated with the input signal. The spectral density of the modulation noise $n_i = e_i - e_{i-1}$ may then be expressed as:

$$N(f) = E(f)\left|1 - e^{-jwT}\right| = 2e_{rms}\sqrt{T}\sin(\omega T/2) \tag{5.59}$$

where $\omega = 2\pi f, T = 1/f_s$ and f_s is the oversampling frequency. In Fig. 5.26, the feedback around the quantizer reduces the noise at low frequencies but increases it at high frequencies. The total noise power in the signal band is:

$$P_n = \int_{-f_B}^{f_B} E^2(f)df = e_{rms}^2 \frac{\pi^2}{3}(2f_B T)^3 = \frac{e_{rms}^2}{OSR^3}\frac{\pi^2}{3} = \frac{\Delta^2\pi^2}{36}\cdot\frac{1}{OSR^3} \tag{5.60}$$

where f_B defines the signal band, and *OSR* is the oversampling ratio. Then the maximum SNR is given by:

$$\begin{aligned} SNR_{\max}[dB] &= 10\log(P_s/P_n) = 10\log\left(3\cdot 2^{2N-1}\right) + 10\log(3\cdot OSR^3/\pi^2) \\ &= 6.02N - 3.41 + 30\log(OSR) \end{aligned} \tag{5.61}$$

Here it can be seen that each doubling of the oversampling ratio of this circuit reduces the noise by 9dB and provides 1.5 bits of extra resolution. The improvement in resolution requires that the modulated signal is decimated to the Nyquist rate with a sharply selective digital filter. Otherwise, the high-frequency components of the noise will spoil the resolution when it is sampled at the Nyquist rate.

5.5.1.4 High order delta-sigma modulator

The objective of using a ΔΣ modulator is to reduce the net noise in the signal band. To do this well, a quantity, whose in-band component is a good prediction of the in-band error, needs to be subtracted from the quantization error. Ordinary ΔΣ modulation subtracts the previous error. Higher order prediction should give better results than this first-order prediction. Fig. 5.26 shows the second-order ΔΣ modulator. It is an iteration of ΔΣ feedback loops. The output of this modulator can be expressed as

$$y[i] = x[i\text{-}1] + (e[i] - 2e[i\text{-}1] + e[i\text{-}2]) \tag{5.62}$$

So the modulation noise is now the second difference of the quantization error. The spectral density of this noise is

$$N(f) = E(f)\left|1 - e^{-jwT}\right|^2 \tag{5.63}$$

and the noise power in the signal band is given by the equation (5.64):

$$P_n = \int_{-f_B}^{f_B} E^2(f)df \approx e_{rms}^2 \frac{\pi^4}{5}(2f_BT)^5 = \frac{e_{rms}^2}{OSR^5}\frac{\pi^2}{5} = \frac{\Delta^2\pi^4}{60}\cdot\frac{1}{OSR^4} \tag{5.64}$$

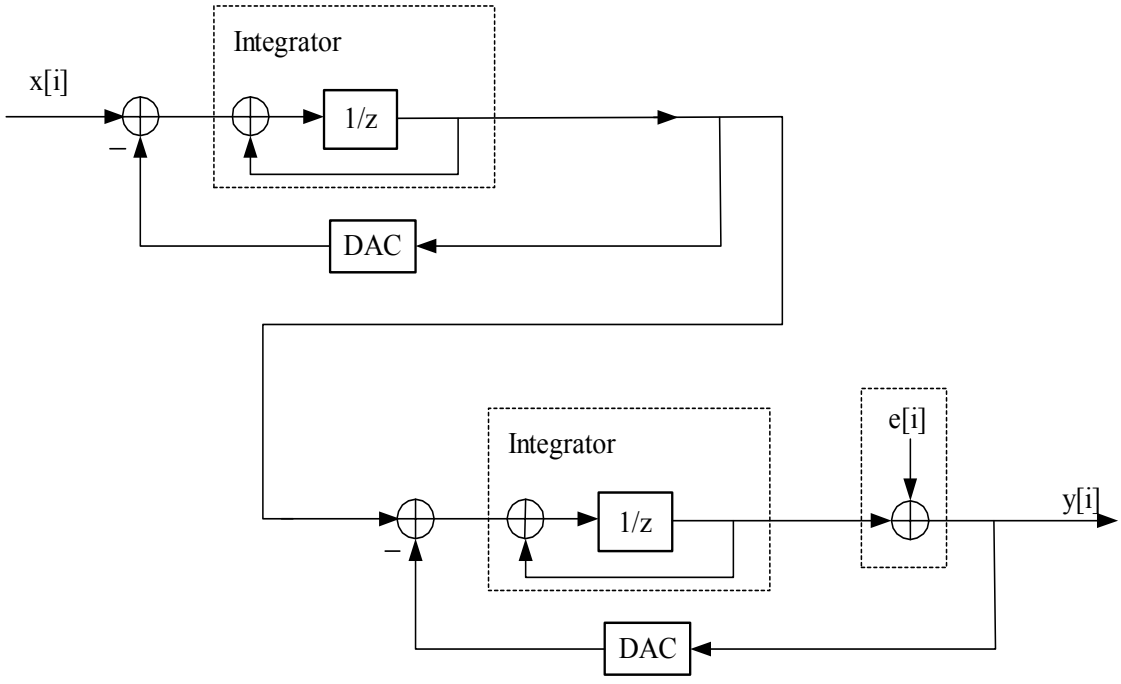

Fig. 5.26: Second order delta-sigma modulator

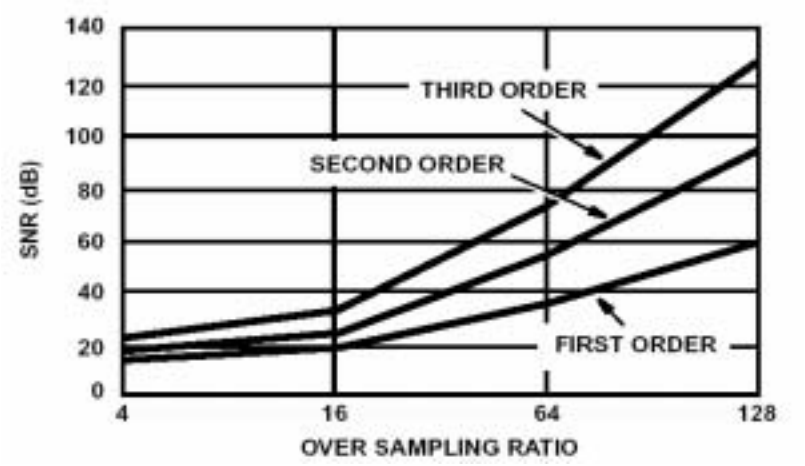

Fig. 5.27: SNR vs. over-sampling ratio for DSM [110]

Then the maximum *SNR* is

$$SNR_{\max}[dB] = 10\log\left(3 \cdot 2^{2N-1}\right) + 10\log(5 \cdot OSR^5 / \pi^4) = 6.02N - 11.14 + 50\log(OSR) \quad (5.65)$$

It can be seen that doubling the OSR improves the SNR for a second-order modulator by 15dB, or equivalently means a gain of 2.5 bits. If the amplitude of the encoded test signal is denoted by A and Δ is the modulator output level, then the SNR is:

$$SNR_{\max} = 15\log_2(OSR) - 11.14 + 6\log_2(A/\Delta) \quad (5.66)$$

In general, the in-band modulation noise of a Delta-Sigma Modulator (DSM) depends on the order of the modulation and the oversampling ratio. For an Lth order DSM, the maximum SNR is given by:

$$SNR_{\max}[dB] = 6.02N + 1.76 - 9.94L + 10\log(2L+1) + 10(2L+1)\log(OSR) \quad (5.67)$$

Fig. 5.27 shows the relationship between the maximum SNR and the oversampling for 1st, 2nd and 3rd order modulation [110]. It is obvious that high SNR values are obtained with high oversampling ratios and high-order quantization. Therefore, there are two approaches to improve the in-band noise property. One is to increase the oversampling ratio and the other one is to increase the order of the modulator. In the first case, a higher oversampling ratio requires more memory on-chip to store the portion of the bit-stream corresponding to a period of the sinusoidal waveform. Hence employing high-order modulators is an efficient alternative to save test hardware on-chip. How-

ever, the stability is the major unanswered theoretical question regarding high-order ΔΣ modulation. It has been shown that high-order modulators can be stabilized. A fifth-order modulator is designed in this method as shown in Fig. 5.28 [72].

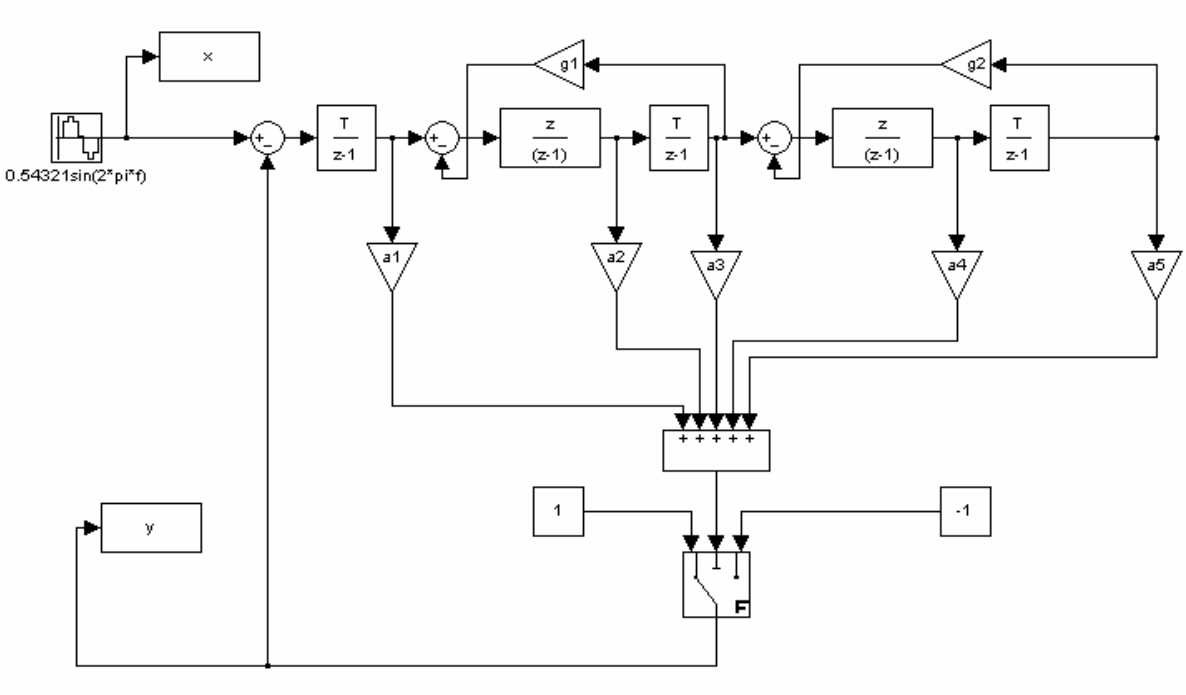

Fig. 5.28: A 5th order delta-sigma modulator

A type of ΔΣ modulator is used, which has a chain of integrators with feed forward summation and local resonator feedback [72]. By adding a small negative-feedback term around the integrators in the loop filter as shown in Fig. 5.28, the open-loop poles can be moved away from dc along the unit circle, which results in the frequencies of infinite loop gain being shifted away from dc to finite positive frequencies. Thus the infinite noise attenuation is able to be moved to the high frequencies. In order to make the modulator stable and get excellent performance of the output bit-stream, the amplifying factors of the fifth-order modulator and the feedback factor must be carefully decided. According to experiences [72], the values of these factors are given and then the modulator is achieved as follows: $a1$=0.56, $a2$=0.25, $a3$=0.054, $a4$=0.0084, $a5$=0.00055, $g1$=0.0007 and $g2$=0.002. The function of the fifth-order ΔΣ modulator can be realized with a C or Matlab program. The optimized portion of the bit-stream and its frequency performance is shown in Fig. 5.29.

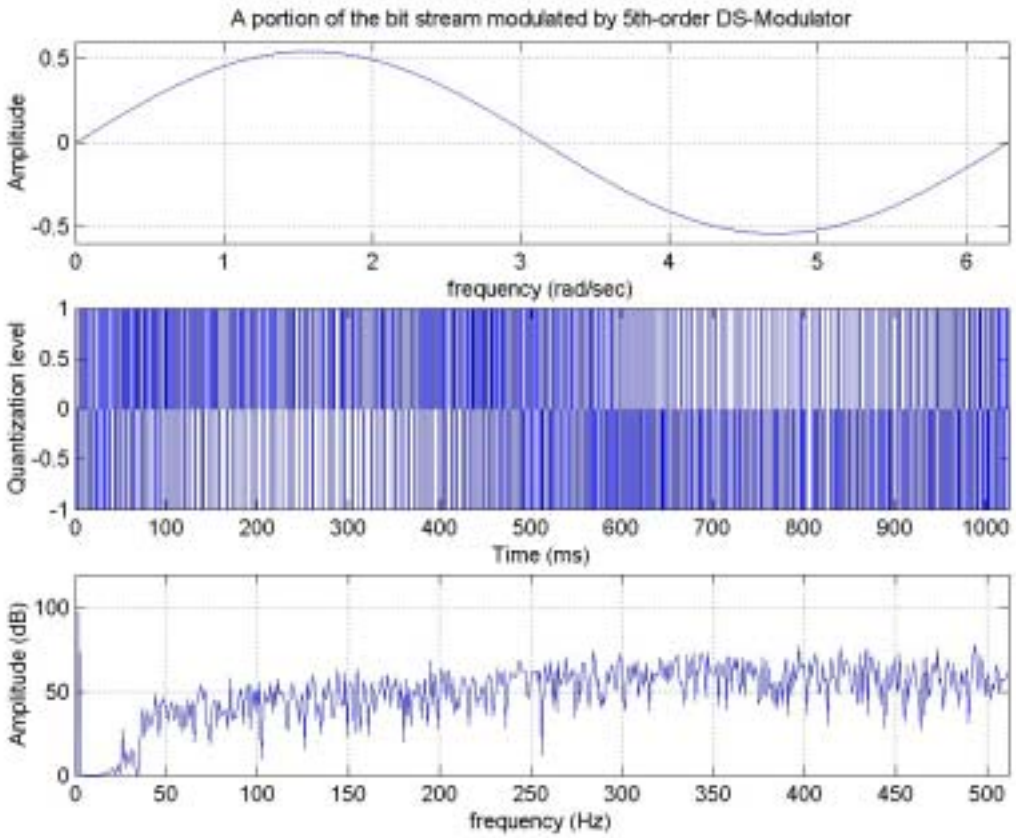

Fig. 5.29: A portion of the bit-stream modulated by 5th-order Delta-Sigma modulator. a) One period sinusoidal signal; b) bit-stream corresponding to a); c) its frequency spectrum

5.5.2 Parameters and performance of the bit stream

It is worth noting that a ΔΣ modulator is a nonlinear component, which means that even the input of the modulator is a periodical signal, its output is still not a periodical one. That is to say, the bit-stream after the ΔΣ modulation is an infinite sequence. But in the case of the BIST, the bit-stream is generated off-chip and only N points of the bit-scream corresponding to an integer number of periods of the sinusoid signal is chosen from the infinite bit-stream and stored in the memory on-chip. After filtered by a LPF these N points of the bit-stream in the memory are repeatedly read out to reproduce the sinusoid signal. With the following conditions, it is stated that the short periodically repeated bit-stream could approximate the output of a 1-bit ΔΣ oscillator very well [39] [40].

Firstly, the repeated frequency for the portion of bit-stream should be harmonically related to the primitive frequency of the bit-stream. There is a relationship between the

length of the portion of bit-stream *N*, the sampling frequency f_s, the period number *M* and the repeated frequency f_o of the portion of bit-stream shown in the equation (5.68):

$$f_o = f_s \frac{M}{N} \tag{5.68}$$

In order to generate a high quality signal, secondly, full periods of sinusoidal stimulus must be modulated. Furthermore, the length of bit-stream *N* has an important influence on the characteristic of the finally generated signal. The larger *N* is, the higher the resolution will be [39]. The minimum N is given by:

$$N_{\min} = 2^{\frac{1}{15}(SNR+23-6\log_2(A/\Delta))} \tag{5.69}$$

where *A* is the amplitude of the encoded test signal and Δ is the modulator output level. At last, it is desirable to run the process of generating the bit-stream for a long time to reach a stable state, then, to select the best sequence available from the bit-stream. The optimizing criterion is dependent upon the application. Here the criterion is based on selecting the minimum amplitude for the total harmonic distortion (THD), while higher harmonic distortions can be filtered out by the LPF.

Chapter 6

Digital Signal Evaluation Procedures

After the generation of the test stimulus is achieved, the second key issue for the built-in self-test is the on-chip measurement of the system's performance. The purpose of the evaluation will be the characterization of the response to the pure tone $x[n] = \cos(2\pi f_0 + \phi)$. The industrial production chains emphasize in particular Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SNDR) and Total Harmonic Distortion (THD). To calculate the THD, the power of the fundamental frequency component f_0 is compared to the power of the harmonic frequency components $2f_0, 3f_0, ..., kf_0$. Note that a discrete signal has a finite number of harmonics k in the positive half-band [0, $f_s/2$). For the SNDR and SNR, the power associated to the fundamental frequency f_0 is compared to the power of all other frequency components in the band [0, $f_s/2$) or all those components except the harmonics.

A reliable routine for the estimation of the value of SNR or SNDR should be developed for evaluating the performance of the method eventually implemented. Another application of this reference method is the computation of the SNR/SNDR value of the sinusoidal stimulus, as explained in Chapter 5.

6.1 Methods relying on the Discrete Fourier Transform (DFT)

It is recognized that the power analyses employing the Fast Fourier Transform (FFT) are the most accurate. The current industrial tests rely heavily on them. In the following section, the estimation of a discrete signal's power using the Discrete Fourier Transform (DFT) will be shown. Essentially, the problem consists in determining an

approximate spectrum $S(\omega)$ estimation or, equivalently, autocorrelation function $R(k)$ estimation of a generic stationary and zero-mean signal x, on the basis of a single realization of L samples $\{x_0, x_1, ..., x_{L-1}\}$.

The power of a zero-mean signal coincides with its variance or, alternatively, the value of the autocorrelation function in the origin: $\sigma^2 = R(0)$. The following average is a statistical estimator of this quantity over L values:

$$\hat{\sigma}^2 = R(0) = \frac{1}{L}\sum_{i=0}^{L-1} x_i^{\,2} \tag{6.1}$$

and it results that it is unbiased:

$$E\left(\hat{\sigma}^2\right) = \sigma^2 \tag{6.2}$$

and consistent (by definition a statistical estimator is unbiased when its expectation coincides with the estimated parameter and it is consistent when its variance goes asymptotically to zero for a growing number of data [63]):

$$\lim_{L\to\infty}\left(E\left[\left(\hat{\sigma}^2 - \sigma^2\right)^2\right] = 0\right) \tag{6.3}$$

This means that for large L the $\hat{\sigma}^2$ computed from a single realization has a high probability of being near the true value σ^2.

Let's now see how these statistical premises can be applied to power estimations. Let $x[n]$ be the signal in the time-domain and $X[k]$ its Discrete Fourier Transform (DFT). According to Parseval's Theorem, the energy of a signal can be computed both from its time-domain and discrete frequency-domain representations:

$$E = \sum_{n=0}^{L-1} x[n]^2 = \frac{1}{L}\sum_{k=0}^{L-1} \left|X[k]\right|^2 \tag{6.4}$$

where L is the length of the sequence. It follows that a signal's power can be computed from the domain as

$$P = \frac{1}{L}\sum_{n=0}^{L-1} x[n]^2 = \frac{1}{L^2}\sum_{k=0}^{L-1} \left|X[k]\right|^2 \tag{6.5}$$

It should be noted that this value is often referred to as the signal's periodogram. Under the assumption of additive noise, the received sequence *y* can be thought of as the superposition of the signal *s* and noise *g*:

$$y[n] = s[n] + g[n] \rightarrow Y(k) = S(k) + G(k) \tag{6.6}$$

So the error can be retrieved from both time and frequency representations. Furthermore, in the presence of a non-correlated signal and noise (zero cross correlation), the powers become additive:

$$P_y = P_x + P_e \tag{6.7}$$

If *L* is the number of collected samples of the received sequence y, then

$$Y(k) = \sum_{n=0}^{L-1} y[n]\, e^{-j\frac{2\pi}{L}kn} \tag{6.8}$$

is the DFT. If the 'analog' frequency ω_0 (of the Fourier transform) corresponds to the 'discrete' frequency k_0 (of the DFT), then

$$\hat{SNDR}\,[dB] = 10\log_{10}\frac{\left|Y(k_0)^2\right|}{\sum_{k=0,k\neq k_0}^{(L-1)/2}\left|Y(k)\right|^2} \tag{6.9}$$

is an estimation of the SNDR. The SNR can be estimated similarly by removing from the total noise the part due to harmonic distortion (the *K* harmonics):

$$\hat{SNR}\,[dB] = 10\log_{10}\frac{\left|Y(k_0)^2\right|}{\sum_{k=0,k\neq k_0}^{(L-1)/2}\left|Y(k)\right|^2 - \sum_{l=1}^{K}\left|Y(l\cdot j)\right|^2} \tag{6.10}$$

An analysis executed in the frequency domain requires a transformation procedure. To compute a Fourier Transform, high computational power should be available, which often is not the case.

In reality, both hardware and software routines require discretized mathematical quantities -- for example, a Fourier transform $x(e^{j\omega})$ can be computed only as a DFT $X(k)$, the latter corresponding to a sampling of the former in the frequency domain. The fre-

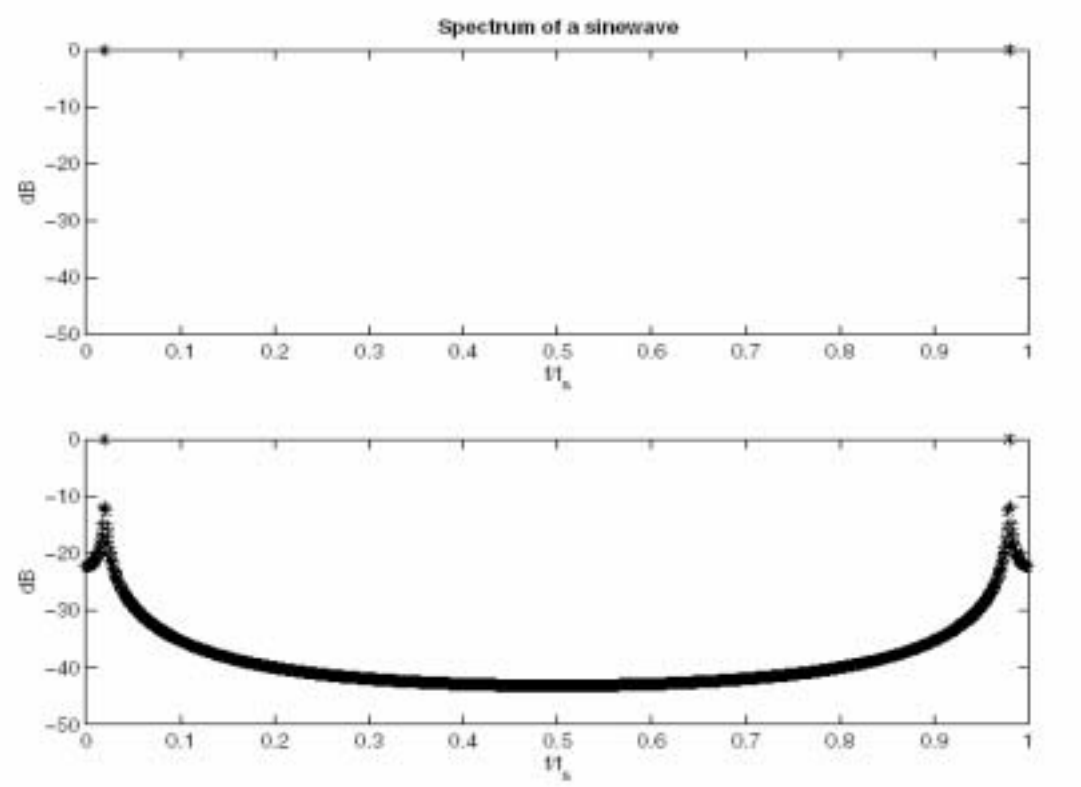

Fig. 6.1: Illustration of the phenomenon of leakage

quency range [0, f_s] is not a continuum anymore because it is divided in L equal subintervals, so that for each of these small bands only one frequency component is considered. The frequency resolution can be increased by taking longer sequences, but to recreate the continuum an infinite sequence would have to be processed, which is obviously impossible. Consequently, the assumption that there exists a discrete frequency j exactly corresponding to the analog frequency ω_0 may not be assured, and instead, a phenomenon known as frequency leakage may appear [63], as illustrated in Fig. 6.1.

For a signal of known frequency, the exact correspondence is easily achieved by selecting L in such a way that a whole number of periods is covered by the samples collected. For generic signals, the leakage is attenuated by windowing. This is done by pre-multiplying the signal with a signal of equal length, which is constructed in such a manner that it attenuates the values toward the borders [63].

Another problem of the periodgram method is that, the larger the number of samples L, or the greater the spectral resolution, the lower the accuracy. This can be circumvented by sectioning the input sequence either in overlapping or in adjacent shorter segments,

taking the periodgram of each and then averaging them to get the final result. This solution was proposed in the 19th century and is still widely used today.

6.2 Least mean squares approximation

A very valuable time-domain method for the signal evaluation is based on the approximation of a noisy sinusoidal waveform using an algorithm that minimizes the mean square error to a clean sinusoidal signal of the same frequency [22] [23]. By assuming that a signal has the type:

$$x[nT] = A\cos(\omega_0 nT) \tag{6.11}$$

and that the output is:

$$y[nT] = \sum_{k=0}^{N} a_k \cos(\omega_0 knT + \phi_k) + g[nT] \tag{6.12}$$

y can be decomposed in a sum of identifiable terms:

$$\begin{aligned} y[nT] = {} & \underbrace{a_0}_{offset} + \underbrace{a_1 \cos(\underbrace{\omega_0}_{signal} n + \phi_1)}_{} \\ & + \sum_{k=2}^{N} \underbrace{a_k \cos(\underbrace{\omega_0}_{harmonics} knT + \phi_k)}_{} + \underbrace{g[nT]}_{noise} \end{aligned} \tag{6.13}$$

The measurements of the quantities of interest are then obtained through ratios of computed powers:

- Total power: $P_y = E[y^2]$
- Signal power: $P_s = a_1^2 / 2$
- Harmonic distortion: $P_h = \left(\sum_{k=2}^{N} a_k^2\right) / 2$
- DC power: $P_{DC} = a_0^2$
- Noise power: $P_g = E[g^2] = P_y - P_s - P_h - P_{DC}$

The equation (6.13) is a system with unknowns a_k, ϕ_k which can be solved by minimizing the mean square error, i.e. the noise power:

$$\min(P_g) = \min(\sigma_g^2) = \min(E[g^2]) \rightarrow (a_k, \phi_k) \tag{6.14}$$

For a finite number of samples collected, the power is substituted by the period:

$$\sigma_\eta^2 = \frac{1}{N}\sum_{n=0}^{N-1} \eta^2[nT] \tag{6.15}$$

This quantity is minimized by constraining the partial derivatives with respect to the a_k and ϕ_k to equal zero and solving the resulting linear system.
Therefore:

$$SNDR = \frac{P_s}{P_g + P_h} \tag{6.16}$$

This method maintains a least mean square solution to estimate the signal. In fact, the present of $y[nT]$ is in the form of Fourier Transform Factor for one frequency point. So the estimate must be unbiased. Compared with FFT which computes the entire spectrum, this approach is computationally more efficient since only the amplitude and phase of the signal and, optionally, the harmonics of interest need to be estimated. Furthermore, windowing of the data is not necessary, even the number of collected samples does not cover an integer number of cycles. However, its application requires a DSP on chip, which limits its application for IC BIST.

6.3 Histogram-based method

The histogram method [24] consists essentially in a counting procedure. When the occurrences of a signal's samples are counted and plotted, a histogram is obtained. If a known signal is applied to a known system, a certain output is expected and, correspondingly, a certain associated histogram. The obtained model histogram can be stored on-chip (for instance, in a ROM). When the real, noisy signal is received at the end of the CUT, a counting operation is performed and stored in a RAM; the obtained results are compared with the expected ones and the test is passed if the magnitude of each code bin falls within acceptable ranges, otherwise it is failed. This method, while needing no more computation than unit increments and comparisons, requires relatively large memories (according to the desired resolution). For example for 16-bit

signals, 2^{16} memory cells are necessary to contain the final number of occurred samples. Furthermore, this test is applicable only to systems in which gain errors don't occur. It is understandable that even a slight change in the signal amplitude, even if the frequency is correct, will cause a totally different distribution of values. For example if a full-scale sinusoidal signal, whose most frequent samples are at the maxima and minima, is reduced in amplitude, the corresponding bins will be empty. By no means can the histogram test be compared to spectral analysis. But it can be run to perform rapid on-chip evaluations of ADCs in systems where a memory is available.

6.4 Pre-defined value and single point DFT methods

Besides the methods proposed above, there are two alternative methods to obtain the SNDR of the tested signal such as pre-defined value method and single point DFT method. By BIST the testing stimulus is generated on chip, which means that the testing signal is pre-detectable. Therefore, some computational efforts can be saved. By assuming that the testing signal is $x(n)$, the response of CUT is $y(n)$ as illustrated in Fig. 6.2, and that there are N sample points in one period, the signal $x(n)$ is able to be predefined. Thus its power P_x can be pre-determined and stored on chip. Then the power of $y(n)$ can be computed by:

$$P_y = \frac{1}{N}\sum_{n=0}^{N-1}\left(y(n)\right)^2 \tag{6.17}$$

Then the value of SNDR can be obtained by:

$$SNDR = \frac{P_x}{P_y - P_x} \tag{6.18}$$

This method is called the pre-defined value approach. It is unbiased if the CUT is a linear component or its sampling rate is kept to a constant. But when the sampling rate of the CUT is not a constant (e.g. decimator), the SNDR value obtained through this method is either underestimated or overestimated.

The pre-defined value method is suitable for the SNDR testing with little hardware requirements that include a small memory on chip to store the power value of the testing stimulus. In addition, the squared-sum function for the extraction of the response

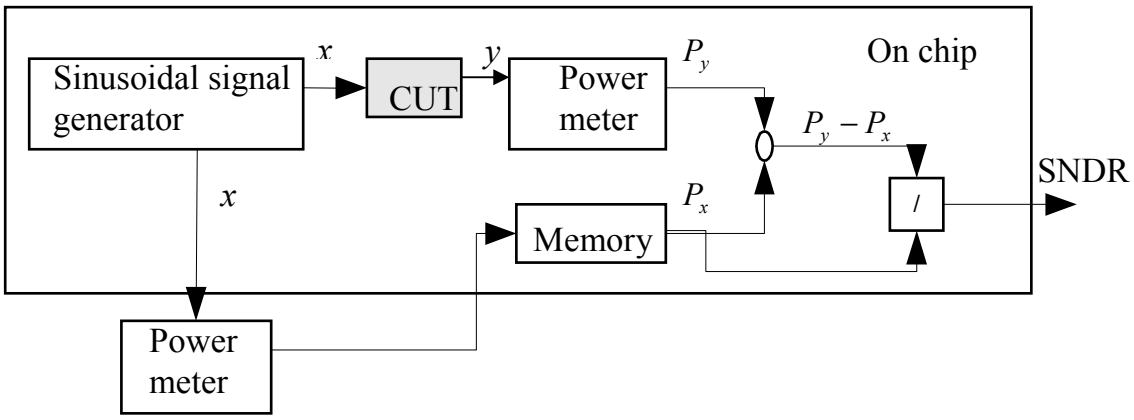

Fig. 6.2: Pre-stored method

power, the subtraction and multiply function should be also available.

Another alternative is the single point DFT method. Assuming there are a signal $y(n)$ and its DFT is $Y(k)$, then:

$$Y(k) = \sum_{n=0}^{L-1} y[n] e^{-i\frac{2\pi}{L}kn}, \quad k = 0,1,\ldots,L-1 \tag{6.19}$$

The distance between two adjacent points in $Y(k)$ equals the frequency resolution of DFT, which is also the sampling rate in the system. If the sampling rate and the desired frequency for the testing are already given, it can be determined which point in $Y(k)$ presents the frequency of interest. Then, instead of a FFT in total frequency band, a single point DFT can be computed.

If sampling rate is f_s and the frequency of interest is f_0, and $k_0 = f_s / f_0$, it follows:

$$Y(k_0) = \sum_{n=0}^{L-1} y[n] e^{-i\frac{2\pi}{L}k_0 n} \tag{6.20}$$

Because this method is based on DFT computation, it is completely unbiased. In addition, this method can also extract the 2nd and 3rd harmonic distortion besides SNDR. Moreover, there must not be DSP on chip, because for a single point DFT only sum and multiplication are needed. So compared with FFT which computes the entire spectrum, this approach is computationally more efficient with a large enough memory on chip to store the sample points. Therefore, this approach can be employed when there is no DSP but some memory available on chip.

6.5 Improved digital notch filter method

The term 'notch filter' usually indicates a highly-selective stop-band (or band-pass) filter, typically used for the removal, extraction or detection of a single tone component from a spectrum. This type of filter has already been adopted in the implementation of BIST applications [37] [38]. If $y(n)$ is the input of notch filter, $s(n)$ and $g(n)$ are the band-pass output and band-stop output of the filter respectively. Then it is very easy to extract the power of *s(n)* and *g(n)*. At last, the division of these two terms is the wanted SNR of $y(n)$. The structure of the filter is shown in Fig 6.3 [37] [38]. There are two outputs: one is band-pass output tuned to the frequency of interest; the other is band-stop output including all the harmonic frequency and noise. $X_{in}(z)$ is the filter input, and $X_{bandp}(z)$ is the band-pass output, while $X_{notch}(z)$ is the band-stop output. The transfer function $H_{bandp}(z)$ from the input $X_{in}(z)$ to the band-pass output $X_{bandp}(z)$ is given by:

$$H_{bandp}(z)=\frac{X_{bandp}(z)}{X_{in}(z)}=-\frac{k_{bw}}{2}\frac{\left(1+z^{-1}\right)\left(1-z^{-1}\right)}{1-\left(2-k_{bw}-k_w{}^2\right)z^{-1}+\left(1-k_{bw}\right)z^{-2}} \tag{6.21}$$

The bandwidth of the band-pass output of the notch filter is determined by the parameter k_{bw}, which is given approximately by $k_{bw}\approx 1-r^2$ (r is the pole radius of the filter). The centre frequency f_0 of the band-pass output is set by the parameter k_w, which is

$$k_w=2\sqrt{1-\frac{k_{bw}}{2}}\sin\left(\frac{\pi f_0}{f_s}\right) \tag{6.22}$$

where f_s is the sampling rate of the filter. And the transfer function $H_{notch}(z)$ from the input $X_{in}(z)$ to the notch output $X_{notch}(z)$ is

$$H_{notch}(z)=\frac{X_{notch}(z)}{X_{in}(z)}=-\frac{2-k_{bw}}{2}\frac{1-\frac{2\left(2-k_{bw}-k_w{}^2\right)}{2-k_{bw}}z^{-1}+z^{-2}}{1-\left(2-k_{bw}-k_w{}^2\right)z^{-1}+\left(1-k_{bw}\right)z^{-2}} \tag{6.23}$$

Equations (6.21) and (6.23) show that both the transfer functions are determined only by k_w and k_{bw}. So the desired transfer functions can be obtained by selecting the values of k_w and k_{bw} carefully. Then the signal and noise can be obtained at the two outputs of the filter respectively. At last it is very easy to extract the power of signal and noise,

and the SNR of the input signal. However, this structure suffers from some problems when it is implemented on chip. One big problem among them is that the transfer functions would be varied when the coefficients (k_w and k_{bw}) are quantified. Moreover, such filter structure is very difficult to be implemented in the form of WDF only with two-port adaptors.

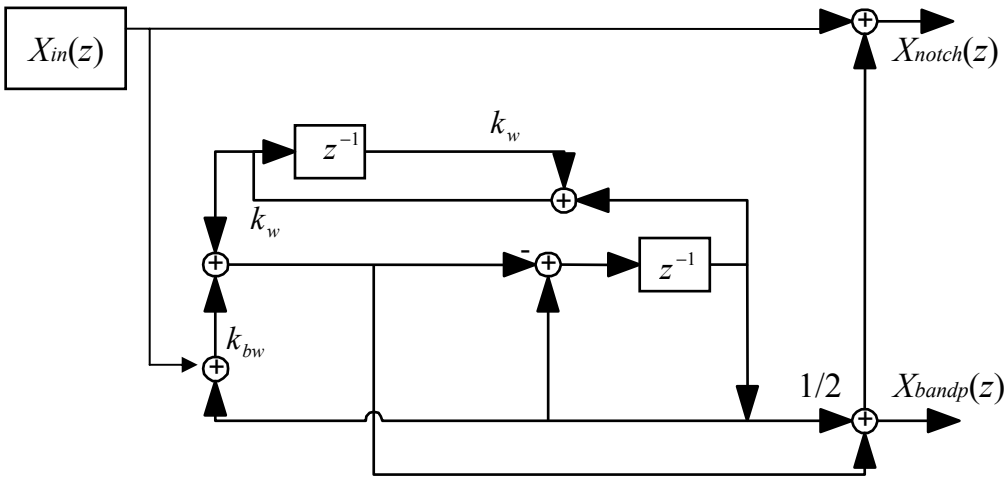

Fig 6.3: Digital notch filter

In this dissertation some improvements will be made on this method so that lattice Wave Digital Filter (WDF) can be employed, whose principles have been introduced in Chapter 4. It is well known that the lattice structure in digital filter design has such character that its transfer function is robust to the variation of the coefficients. So the coefficients quantization error has the smallest effect on the performance of the filter compared with other filter structures such as direct form I or direct form II [63].

Moreover, wave digital filter has some notable properties [64] [65] [67] [68] [70]: excellent stability properties — WDF can still maintain stable even under nonlinear operating conditions which result from overflow and round-off effects, low coefficient word-length requirements, good dynamic range, etc. All these advantages are a consequence of the fact that WDF's behave completely like passive circuits, if properly designed. This can be found in Chapter 4. Now a brief development to the lattice WDF notch filter structure will be given, which is summarized from [63] [69] [73]. The transfer function of an analog notch filter [73] is given as

$$H(s) = \frac{s^2 + \lambda^2}{s^2 + bs + \lambda^2} \tag{6.24}$$

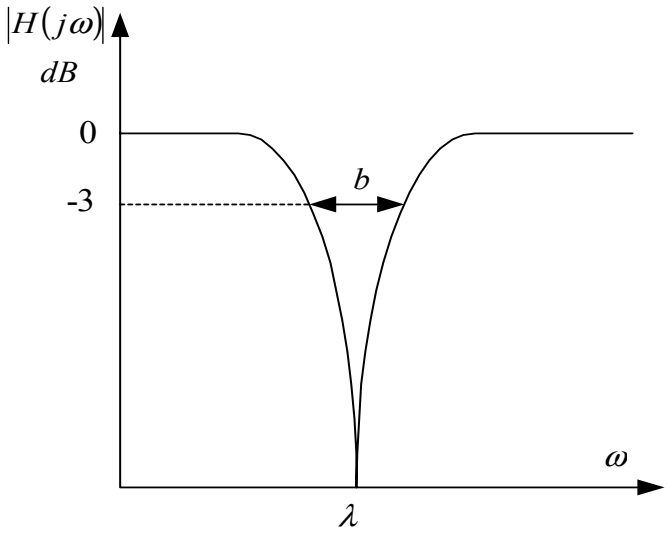

Fig. 6.4: Notch filter for the continuous case

Its magnitude function $|H(j\omega)|$ is sketched in Fig. 6.4, which shows that the *dc* gain of this filter is 0 dB and $\omega = \lambda$ is the notch frequency at which there is no transmission through the filter. Within the frequency band centered at $\omega = \lambda$ and of width *b*, all the signal components are attenuated at least 3 dB. Thus the 3-dB refection bandwidth of this filter is *b*.

Applied the bilinear transform $s = (z\text{-}1)/(z\text{+}1)$ [63] to $H(s)$, equation (6.25) can be yielded:

$$H(z) = \frac{(1+\lambda^2) - 2(1-\lambda^2)z^{-1} + (1+\lambda^2)z^{-2}}{(1+\lambda^2+b) - 2(1-\lambda^2)z^{-1} + (1+\lambda^2-b)z^{-2}} \tag{6.25}$$

With

$$a_1 = \frac{2(1-\lambda^2)}{1+b+\lambda^2}, \quad a_2 = \frac{1-b+\lambda^2}{1+b+\lambda^2} \tag{6.26}$$

the transfer function $H(z)$ can be expressed in a different form and with minimum number of the coefficients as:

$$H(z) = \frac{1}{2} \cdot \frac{(z^{-2}+1) - 2a_1 z^{-1} + a_2(z^{-2}+1)}{1 - a_1 z^{-1} + a_2 z^{-2}} \tag{6.27}$$

Because $z = e^{j\omega T}$ and the *dc* gain can be obtained by letting $z = 1$, the *dc* gain of the $H(z)$ is 1 (or 0 dB). The magnitude function of $H(z)$ is noted as $|H(j\omega T)|^2$ and given by

$$|H(j\omega T)|^2 = \frac{\left[\left(1+\lambda^2\right)\cos(\omega T)-\left(1-\lambda^2\right)\right]^2}{\left[\left(1+\lambda^2\right)\cos(\omega T)-\left(1-\lambda^2\right)\right]^2 + b^2\sin^2(\omega T)} \tag{6.28}$$

The notch frequency ω_0 is obtained, if the numerator is equal to zero, which yields

$$\cos(\omega_0 T) = \frac{1-\lambda^2}{1+\lambda^2} \quad \rightarrow \quad \omega_0 = \frac{1}{T}\cdot\arccos\left(\frac{1-\lambda^2}{1+\lambda^2}\right) \tag{6.29}$$

Furthermore, the frequencies ω_1 and ω_2 where the magnitude is attenuated 3 dB from its *dc* value determine the 3-dB-bandwidth and can be obtained by solving

$$\left[\left(\lambda^2+1\right)\cos(\omega T)-\left(1-\lambda^2\right)\right]^2 = b^2\cdot\sin^2(\omega T) \tag{6.30}$$

which yields that

$$\begin{aligned} &\cos(\Omega T) = \cos(\omega_1-\omega_2)T = \frac{\left(1+\lambda^2\right)^2 - b^2}{\left(1+\lambda^2\right)^2 + b^2} \\ &\rightarrow \quad \Omega = \frac{1}{T}\cdot\arccos\left(\frac{\left(1+\lambda^2\right)^2 - b^2}{\left(1+\lambda^2\right)^2 + b^2}\right) \end{aligned} \tag{6.31}$$

Thus λ^2 and b^2 can be solved as a function of ω_0 and Ω, which means the constant a_1 and a_2 are also the functions of ω_0 and Ω. Then :

$$\begin{cases} \lambda^2 = \tan^2\left(\dfrac{\omega_0 T}{2}\right) \\ b = \left(1+\lambda^2\right)\tan\left(\dfrac{\Omega T}{2}\right) \end{cases} \rightarrow \begin{cases} a_1 = \dfrac{2\cos(\omega_0 T)}{1+\tan(\Omega T/2)} \\ a_2 = \dfrac{1-\tan(\Omega T/2)}{1+\tan(\Omega T/2)} \end{cases} \tag{6.32}$$

It is worth noting that the notch frequency ω_0 can be changed while keeping the 3-dB rejection band and *dc* gain constant just by changing a_1. Similarly, the rejection band-width Ω can only be varied by selecting a proper value of a_2. However, to keep the notch frequency invariant, a_1 should be adjusted accordingly.

In the case of realization of the transfer function of the notch filter, an all-pass filter with lattice structure is employed. To explain this point more clearly, the equation (6.27) is rewritten here as:

$$H(z)=\frac{1}{2}\cdot\frac{\left(z^{-2}+1\right)-2a_1z^{-1}+a_2\left(z^{-2}+1\right)}{1-a_1z^{-1}+a_2z^{-2}}=\frac{1}{2}\cdot\left(1+\frac{a_2+\left(1+a_2\right)\cdot\frac{-a_1}{1+a_2}z^{-1}+z^{-2}}{1+\left(1+a_2\right)\cdot\frac{-a_1}{1+a_2}z^{-1}+a_2z^{-2}}\right) \tag{6.33}$$

Introducing the intermediate sequence $A(z)$ by

$$A(z)=\frac{a_2+\left(1+a_2\right)\cdot\frac{-a_1}{1+a_2}z^{-1}+z^{-2}}{1+\left(1+a_2\right)\cdot\frac{-a_1}{1+a_2}z^{-1}+a_2z^{-2}} \tag{6.34}$$

there is

$$H(z)=\frac{1}{2}\cdot\left(1+A(z)\right) \tag{6.35}$$

Obviously, $A(z)$ represents a 2nd order all-pass filter [63] [69], whose transfer function is expressed as the ratio of two polynomials with conjugate reciprocal zeros and poles. Then the realization of the notch filter is shown in Fig. 6.5.

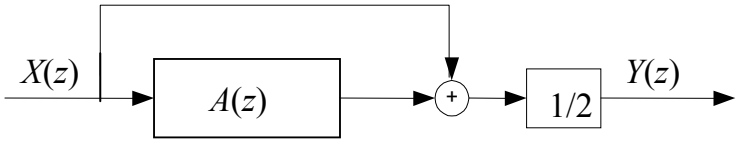

Fig. 6.5: Implementation of the digital notch filter

Since A(z) is a 2nd – order all-pass filter, the change in phase of $A\left(e^{j\omega}\right)$ is -2π radians as ω goes from 0 to π. And for the transfer function of the notch filter $H(z)$, it follows:

$$\begin{cases}H\left(e^{j0}\right)=H\left(e^{j\pi}\right)=1\\H\left(e^{j\omega_0}\right)=0\end{cases} \tag{6.36}$$

In the equation (6.36), ω_0 is the angular frequency at which the all-pass filter provides a phase shift of π radians. Provided $A(z)$ is realized in a structurally lossless form, the characteristic of the notch filter is structurally induced. A particularly usefully structure for the 2nd order all-pass filter is a lattice filter which is illustrated in Fig. 6.6,

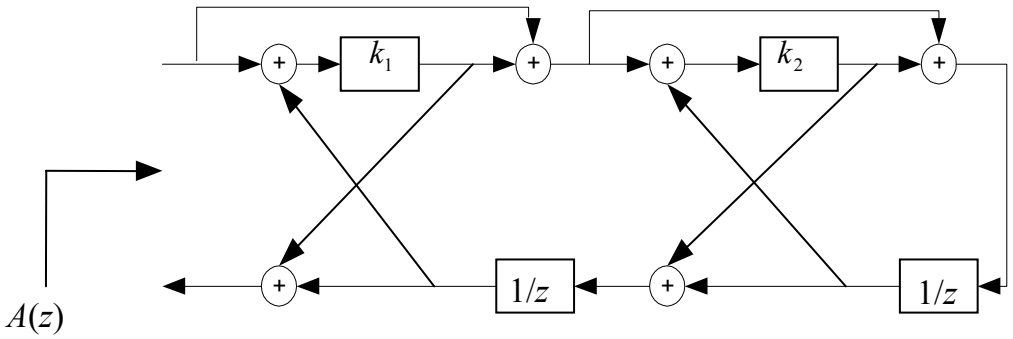

Fig. 6.6: Implementation of all-pass filter

where $k_1 = a_2$ and $k_2 = -a_1/(1+a_2)$. Fig 6.7 shows the typical appearance of the transfer function of the notch filter. The dependence of the selectivity on the parameter a_2 (namely k_1) is also illustrated.

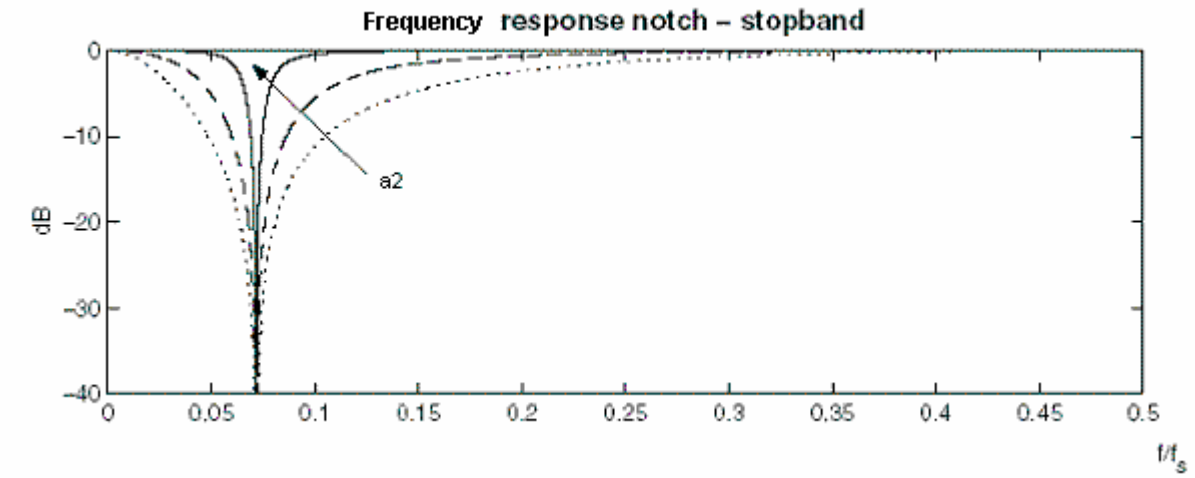

Fig. 6.7: Transfer function of notch filter

This notch filter is a band-stop filter. After filtering, the signal is attenuated from the input signal, and the noise in band is outputted with the distortions together. Removing these frequency components (noise + distortions) from the original input waveform, the signal can be reconstructed. Then the signal and noise can be obtained respectively. Finally, with additional functional blocks, the SNDR value of the input can be computed. An interesting modification to the circuit in Fig. 6.5 results through replacing the delay variable z^{-1} by z^{-N}. The circuit then provides N complex-conjugate zero pairs along the unit circuit, located at angles of

$$\frac{2\pi n \pm \omega_0}{N}, \qquad n = 0,1,\cdots,N-1 \tag{6.37}$$

Such a filter can attenuate *N* frequency components in the input signal. By selecting this *N* zeros carefully, the signal and its distortion can be removed from the input. Detailed information can be found in [69]. Therefore, the SNR value instead of the SNDR value can be computed finally. In other words, the digital notch filter is able to be used to obtain both SNDR and SNR values.

A highly selective notch filter, tuned to totally cancel out the fundamental frequency of the sinusoidal waveform, leaves in principle just the noise and distortion products. This method is rather inexpensive and yet precise, as a second order filter is already very selective and it is not necessary to go beyond the fourth order. Moreover, a deep notch filter would require a long settling time.

It may be seen that if a noisy sinusoidal signal consisting of white noise and a single tone is passed through the band pass, some of the noise will pass through due to the finite bandwidth of the filter. Then it will be tailed with the signal power, resulting in an overestimation. In addition, the notch filter removes some of the noise power with the result that noise power is underestimated. The net result is that the estimation SNDR based on notch filter is indeed slightly higher than the true SNR.

This method yields a biased estimation of SNR. In addition, it is necessary to wait for the filter to reach steady state before initiating the measurement. It is also reported that, when the desired precision is increased, the necessary time to wait for the notch filter to reach steady state also increases [37] [38]. However, if the pole locations of the filter are chosen properly, the bias can be made very small and the settling time can be made tolerable. The amount of precision required for the coefficients will affect the choice of the number of bits used for the arithmetic in the filter, which will affect the silicon area needed to build in hardware.

The choice of notch filter based on all-pass structures is particularly fortunate for application to the case of WDF. From above, the filter is already expressed as sum of two all-pass filters, $A(z)$ and 1, which automatically make up the two branches of a lattice WDF. Recalling the contents about the design of a 2nd order all-pass wave digital filter described in Chapter 4, one conclusion is able to be drawn immediately : $r_1 = -k_1$ and $r_2 = -k_2$.

Moreover, the guard-bits must be added to prevent the overflow and the rear-bits to get rid of the round off noise in the notch filter. For a 2nd order notch filter, two guard-bits are normally enough to eliminate the overflow error inside the filter. Due to the WDF structure described in Chapter 5.4.9, the selection of rear-bits is somewhat complex. It

must be at least "1" if there is a click-clack signal for this adaptor. Moreover, it should equal to the scaling factor of this adaptor, if there is such a factor. The scaling factor represented by r here is included in the coefficients. In second order sections it may happen in fact that the signal leaving the first block and entering the second is too small. This can happen when the coefficient of the first adaptor is very small. Consequently, when entering the second adaptor, the right shifts in the shift-and-add multiplication reduce the signal even more, increasing the risk of limit cycles. An optimal scaling factor can be calculated for each all-pass section from the two coefficients and is then approximated as a power of two, namely 2^r. The coefficient is scaled up by this quantity. After the multiplications the signal is scaled down again to retrieve the correct value. This allows a better utilization of the bits available. The rear-bits lie in such a range as [1, $max(r)$]. And there will be $max(r) = 4$ by the implementation of notch filter in WDF, if the filter degree does not exceed two.

There are also other factors which contribute to the degradation of the filter's performance. The coefficient quantization error is one of the most important factors. It causes the change of the transfer function of a system. And such change would perhaps give rise to the degradation of the system's character. So the simulation is made to show how the quantization resolution of the coefficients affects the attenuation ability of the notch path. Because the signal is estimated by removing the noise (the output of the notch path) from the total signal, the maximum SNR that the notch path can attenuate is the processing limitation of the digital notch filter. The results are given in Fig. 6.8 and Fig. 6.9. Fig. 6.8 shows that the limitation (SNR) of the notch filter increases when the quantization bits of the coefficients become bigger, and Fig 6.9 shows that the variation of the notch frequency decreases when the bit number increases. By both figures there is a notch frequency of 0.05 normalized to sampling frequency, namely $f_s = kf_0 = f_0 / 0.05 = 20 f_0$, and k is called as the sampling ratio of this digital system. In order to exam whether the notch frequency (normalized to sampling rate), or the sampling ratio, affects the system's performance or not, the following simulation is performed. By setting the bit number to 20, the notch frequency varies from 0 to $0.05 f_s$. The processing limitation of the digital notch filter is measured and illustrated in Fig. 6.10. This figure shows that the notch filter reach its maximum attenuation ability at the normalized notch frequency in the range of [0.049, 0.436]. In other words, this range is the optimal working range of the notch filter. It is suggested that the working range be in the first half range [0.049, 0.25]. The reason is that, on the one hand, the sampling rate of the filter in the first half range is higher than that in the other half range. This results in more design efforts and power dissipation on chip; but on the other hand, the processing speed increases, which makes the testing time much shorter.

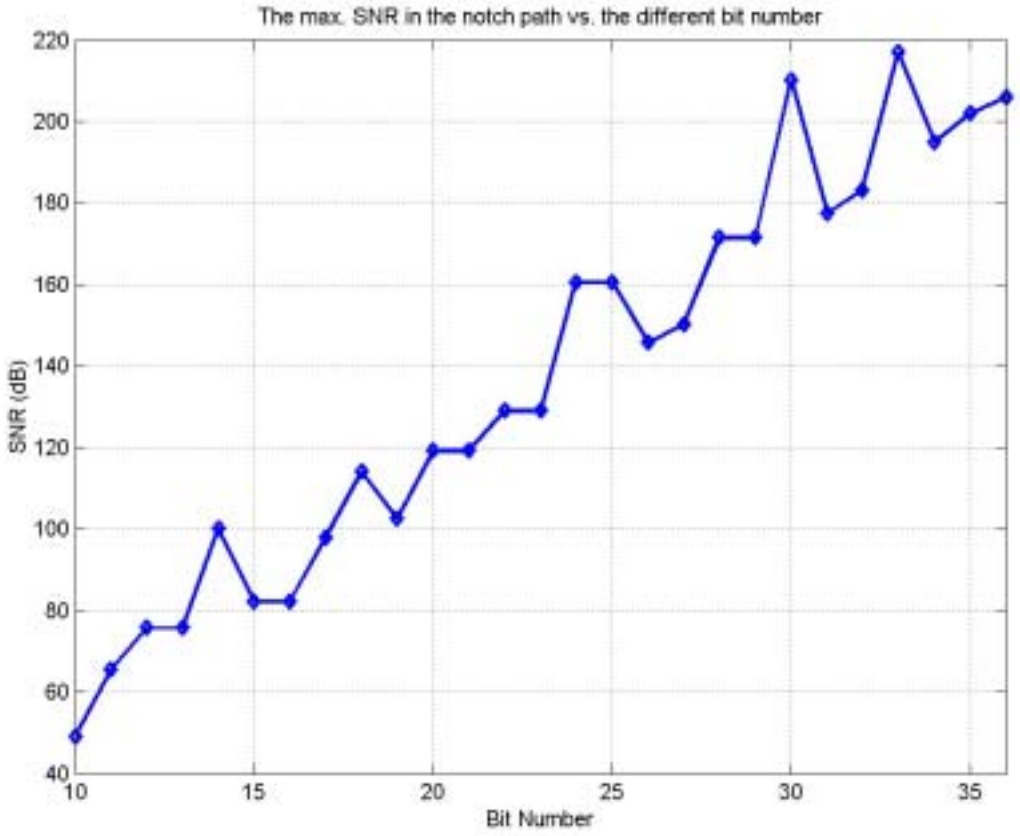

Fig. 6.8: The limitation of the max. SNR

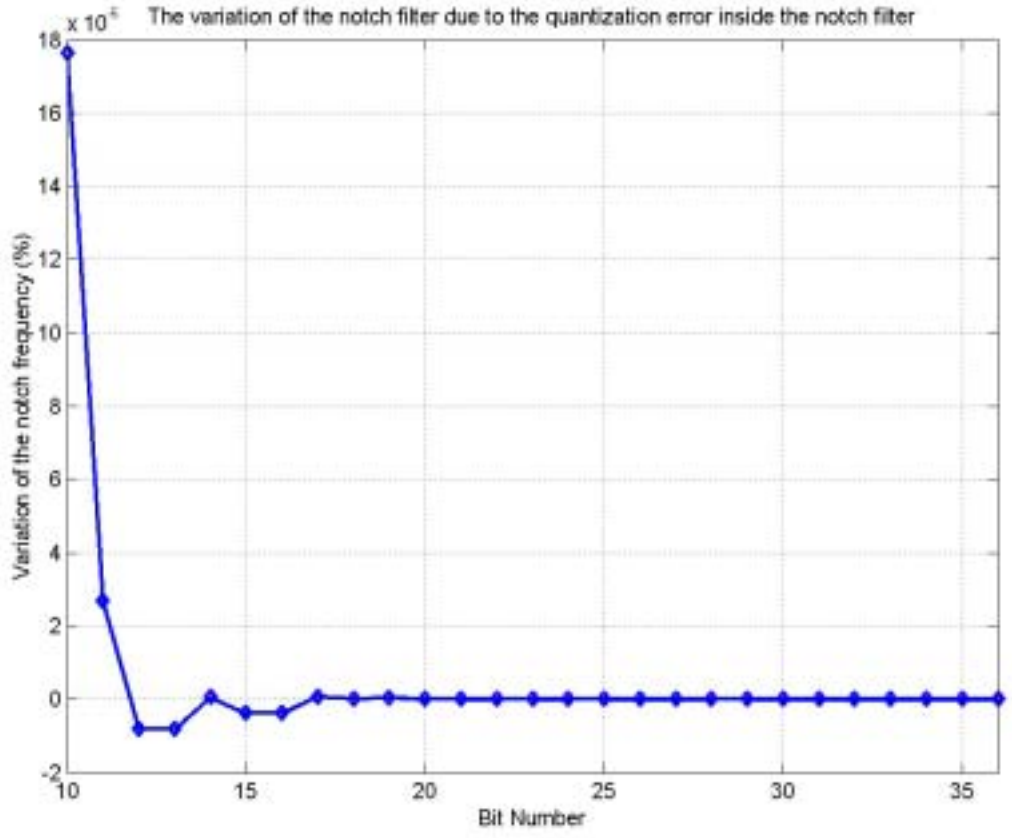

Fig. 6.9: The variation of the notch frequency

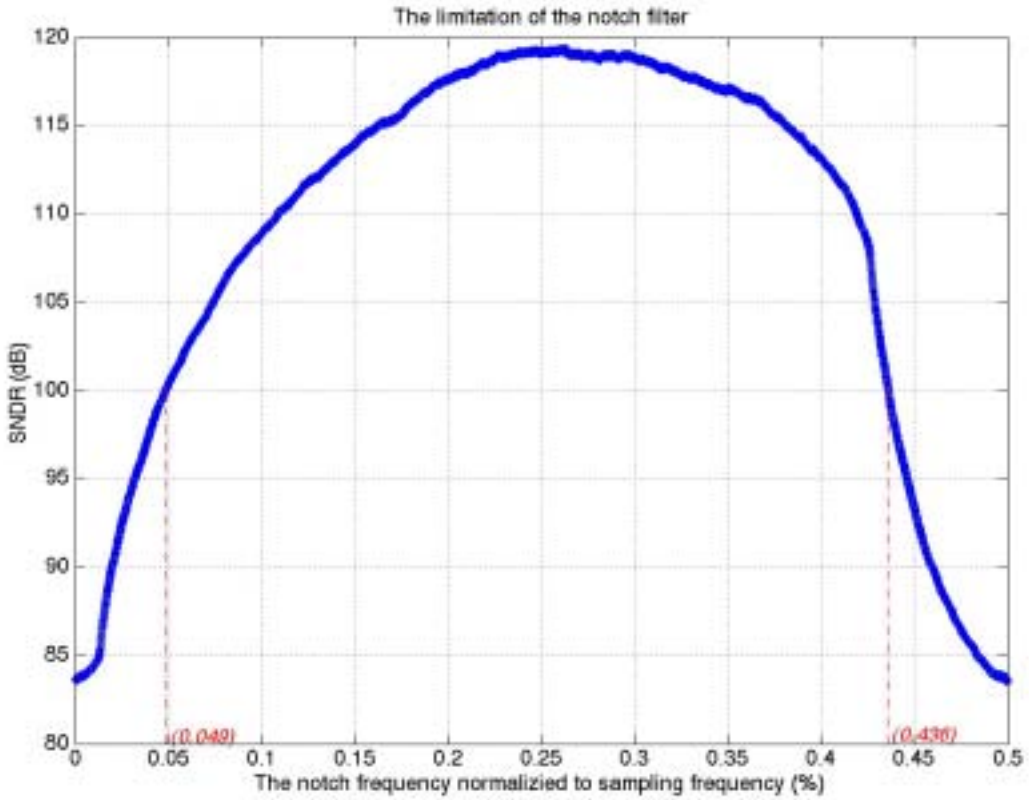

Fig. 6.10: The limitation of the notch filter

Chapter 7

Implementation of the Test Concept

In Chapter 3, a new BIST method for the ADC/DAC pairs, so-called Loop-BIST, has been introduced, and the detailed algorithms of the three different cases for the Loop-BIST have also been described: the resolution of ADC is equal to that of DAC, which is denoted by C1 (Case 1); the resolution of ADC is smaller than that of the DAC, which is denoted by C2 (Case 2); and the resolution of the ADC is greater than that of the DAC, which is denoted by C3 (Case 3). Various on-chip signal generation methods as well as some approaches for measuring the response on chip have been summarized in Chapter 4, Chapter 5 and Chapter 6. In this chapter, the implementations and the simulations of the concept will be given. At the end of this chapter, the testing of one special case – the Loop BIST for DAC/ DELTA-SIGMA ADC pairs – will be discussed. First of all, a brief introduction of the implementation and simulation environment is present as follows..

7.1 Implementation and simulation environment

To verify the correctness of the design, simulations and implementations have been carried out in the MATLAB and COSSAP environments, and in some cases other tools such as ModelSim, Design Compiler are also used. In this section, we will make a brief introduction to the key simulation and implementation tools – Matlab and COSSAP. Appendix B includes a more detailed description about COSSAP and a brief description about ModelSim and Design Compiler.

Matlab (**Mat**rix **lab**oratory) is an interactive software system for numerical computations and graphics. As the name suggests, Matlab is especially designed for matrix

computations: solving systems of linear equations, computing eigenvalues and eigenvectors, factoring matrices, and so forth. In addition, it has a variety of graphical capabilities, and can be extended through programs written in its own programming language. Many such programs come with the system; a number of these extend Matlab's capabilities to nonlinear problems, such as the solution of initial value problems for ordinary differential equations.

Matlab is one of the fastest ways to solve problems numerically. The computational problems arising during the algorithm design can be solved much more quickly with Matlab, than with the standard programming languages (FORTRAN, C, Java, etc.). It is particularly easy to generate some results, draw graphs to display the interesting features, and further explore the problem. By minimizing human time, Matlab is particularly useful in the initial investigation of real problems. It is a system design tool tailored for software simulations. More information about Matlab can be found in [94] – [97].

COSSAP represents a system-level design environment for the implementation of complex digital signal processing and communication systems. As a hardware design tool, it reproduces the real execution of the algorithm as it will be implemented. Furthermore, the realization of a test-bench in COSSAP was necessary for two practical reasons. Firstly, it allows a global verification of the BIST's effectiveness, since in some cases the components of the codec chip under test have been previously realized as COSSAP models; secondly, the tool allows an estimation of the area and power consumption claimed by the concept.

7.2 Implementation of Loop-BIST for C1

7.2.1 Circuit under Test (CUT)

The CUT is a voice-band coding part (often referred to simply as codec) in a GSM/UMTS front end chip, whose block scheme is shown in Fig. 7.1. Two opposite paths dedicated to different tasks are distinguished: the one on the D/A (digital to analog) line outputs the incoming signal to the loudspeaker; the other one, on the A/D (analog to digital) line, sends the voice sampled from the microphone to the antenna.

The path to the earpiece contains digital interpolation filters, a digital-to-analog con-

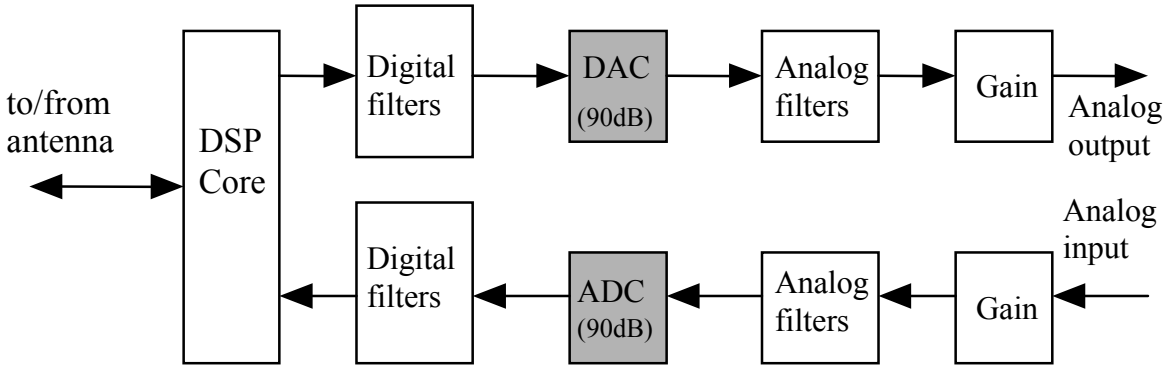

Fig. 7.1: Block scheme of the GSM/UMTS front-end

verter (DAC) and analog post filters. The incoming signals can represent different types of sound voice mono, voice stereo, music stereo and have therefore different sampling frequencies (fs= 8, 16, 32, 44.1, 48kHz). The DAC, on the other hand, operates at a fixed frequency of 4MHz with a SNR equal to 90 dB, so that the bank of interpolation filters is necessary to align the different rates. The interpolation filters also cause over-sampling of the signal, which reduces the complexity and the cost of the required analog reconstruction filters following the converter.

The path from the microphone consists of an analog anti-aliasing filter, an analog-to-digital converter (ADC) and digital decimation filters. This time the analog signal is (over)sampled by a 2MHz ADC with a same SNR as that of DAC (90 dB). This signal needs to be translated to the typical voice-band rates of 8 kHz and 16 kHz, so that decimation is applied. The converter's band is smaller because only voice and no music is transmitted uplink.

The multi-rate filters for both interpolation and decimation are implemented on an embedded application-specific digital signal processor. It is highly optimized for sampling rate conversion operations, so-called ASMD (Application-Specific Multi-rate Digital signal processor) [79], and specifically designed to run a particular class of filters known as wave digital filter, as introduced in Chapter 4. Consistently with the effort of circuit reconfiguration, the ASMD will be used to run the (wave-digital) filter necessary for this concept.

7.2.2 Loop BIST Structure

The resolution of the ADC in this scheme is the same as that of the DAC. The Loop-BIST algorithm and scheme were described in Chapter 3.3.3 and Fig. 3.8 respectively.

The strategy is to short-circuit the receiving and the transmitting paths on the analog side in test mode so that the looped circuit appears fully digital. The signals necessary for the functional tests of the on-chip components are generated with the aid of the ASMD and as little extra hardware as possible. They are then applied to the digital-to-analog converter and fed into the loop. After sampling with the analog-to-digital converter, the received signals are again evaluated using digital signal processing methods on the ASMD. This way it is verified if the performance of the analog components falls within the specification limits.

Then this system needs one 1.5 kHz digital sinusoidal stimulus with the SNR above 90 dB and one digital signal evaluator, whose implementation methods have been described in Chapter 5 and Chapter 6, respectively. The approach based on filtering a periodic signal described in Chapter 5.4 is used to produce the 1.5 kHz testing stimulus. The digital notch filter in Chapter 6.5 is adopted as the on-chip signal evaluator in this Loop BIST structure, whose notch frequency is 1.5 kHz and attenuation at the notch frequency is at least 90 dB. In both generation and evaluation schemes a wave digital realization of the filters involved allows them to be implemented on the available digital signal processor (the ASMD). The detailed design issues of the WDF were presented in Chapter 4.

Table 7.1: The parameters of the design

Quantity	**Value**
f_{s1}	800 kHz
INC	65
N	14
DEC	25
f_{s2}	32 kHz
f_0	1.5869 kHz
S	5461
K	2

For the design of on-chip digital sinusoidal signal generator, the parameters described in Chapter 5.4 are set as the values in Table 7.1. It should be noted that in the implementation of low pass filter the sampling frequency of the filter could be decimated exactly to the target rate of the DAC of 4 MHz. However, the specifications on a low pass filter of pass band around 4-6 kHz and normalized half-band of 2MHz will be-

come extremely tight. It is actually possible to implement them with a 5^{th} or 7^{th} order WDF based on a Cauer analog model. But the problem is that such filter is unrealizable in fixed-point arithmetic, because only the coefficients' quantization requires some 19-20 bits to maintain the specifics. This results in an overly long signal word length. Besides, the tight transition band would cause a very long transient on the output. Then the advantages gained by the faster clock would be lost in waiting time and extremely long registers. The implemented low pass filter operates at 32 kHz and requires, at the most, 11 bits for its coefficients.

7.2.3 Simulation results

The system has been implemented under COSSAP environment. The simulation results are given in this section. At first, the generation of the sinusoidal waveform is simulated under COSSAP environment. The values of design parameters are from Table 7.1 in Chapter 7.2.2. Because there is a total of 80000 samples in the simulation results, it is impossible to display them clearly in a figure. Hence Fig. 7.2 gives only a portion of the produced trapezoid waveform, which will be given into the low pass filter to remove the higher frequencies. It is obvious that the ramps are as long as the floors in Fig. 7.2, which leads to the fact that the 3^{rd} harmonic distortion disappears completely. This relaxes the design of the low pass filter. After the calculation a value of SNR = 59.50 dB is obtained. Then we make the simulation of low pass filter, whose transfer function is shown in Fig. 7.3. The filter operates at 32 kHz and needs, at most, 11 bits for its coefficients. Its cut-off frequency lies at 1.6 kHz and the transient band lies between 1.7 kHz and 4 KHz. It is stated that a 1.5 kHz sinusoidal waveform is adopted for the testing stimulus (Chapter 7.2.2). The first undesired frequency that the low pass filter should eliminate is the 5^{th} harmonic frequency, since the amplitude of the 3^{rd} harmonic frequency disappears from the spectra. Fig. 7.3 illustrates that the attenuation of the filter can filter out all the frequencies after 5x1.5 = 7.5 kHz, which means that this low pass filter is able to remove all the harmonic distortion. After the filtering, only fundamental frequency is kept and outputted, which is the final sinusoidal waveform illustrated in Fig. 7.4. Of course, the SNR value of the final signal is improved through filtering the higher harmonic distortions in the trapezoid wave. The final achievable SNR is 96.15 dB. Since the performance of the signal generator is better than that of the CUT, this generation approach is suitable for the BIST application. It should be noted that the system can only reach its stable output after some settling time and that the first *M* samples of output should be eliminated by practical application. Obviously, the value of *M* determines not only the SNR of the finally produced

testing stimulus but also the total testing time. So the variation of the SNR of the testing signal with different *M* is simulated in this work. The results are given in Fig. 7.5 and Table 7.2.

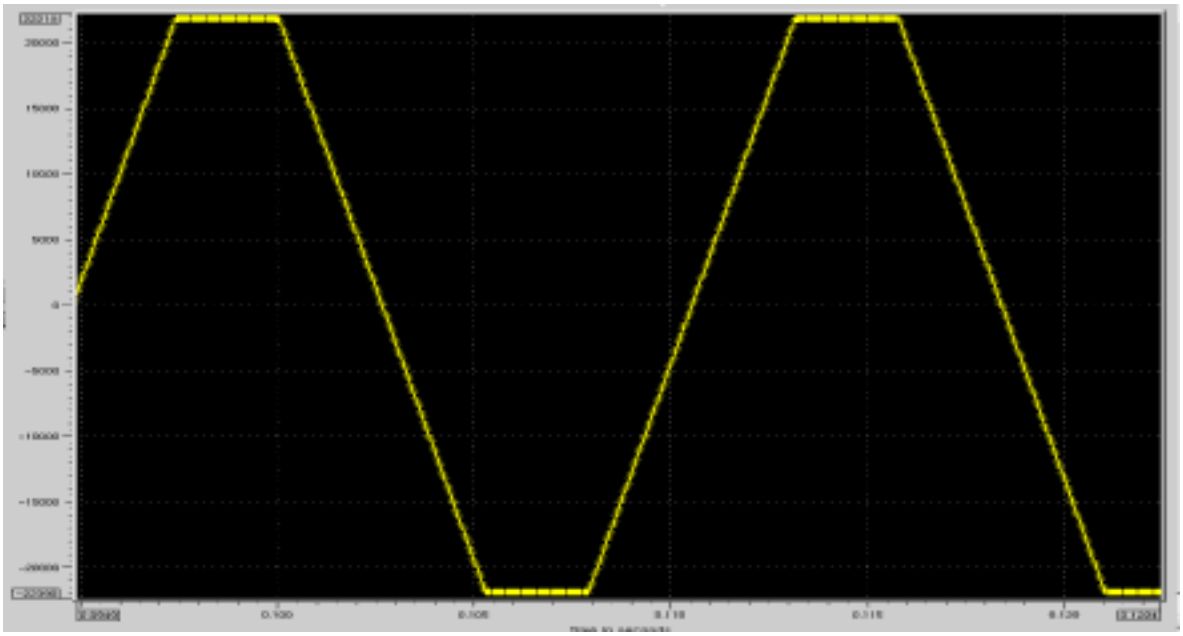

Fig. 7.2: Trapezoid waveform with SNDR = 59.50 dB

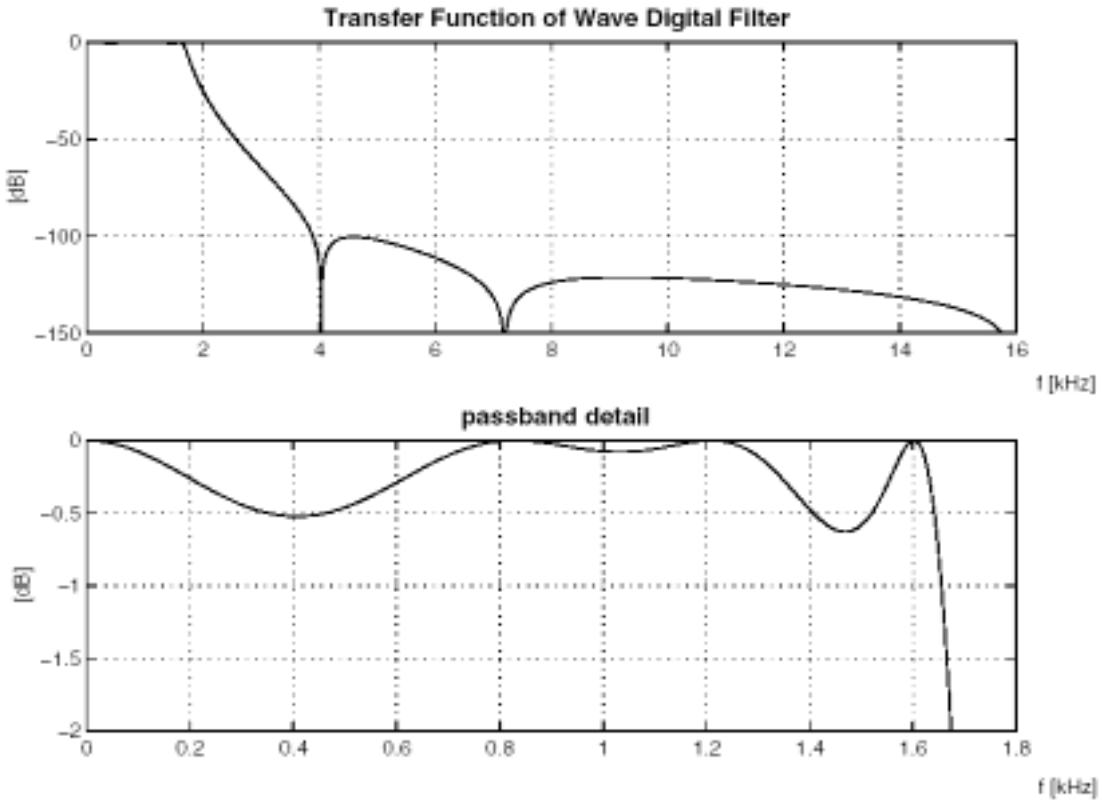

Fig. 7.3: Transfer function of the implemented wave digital filter

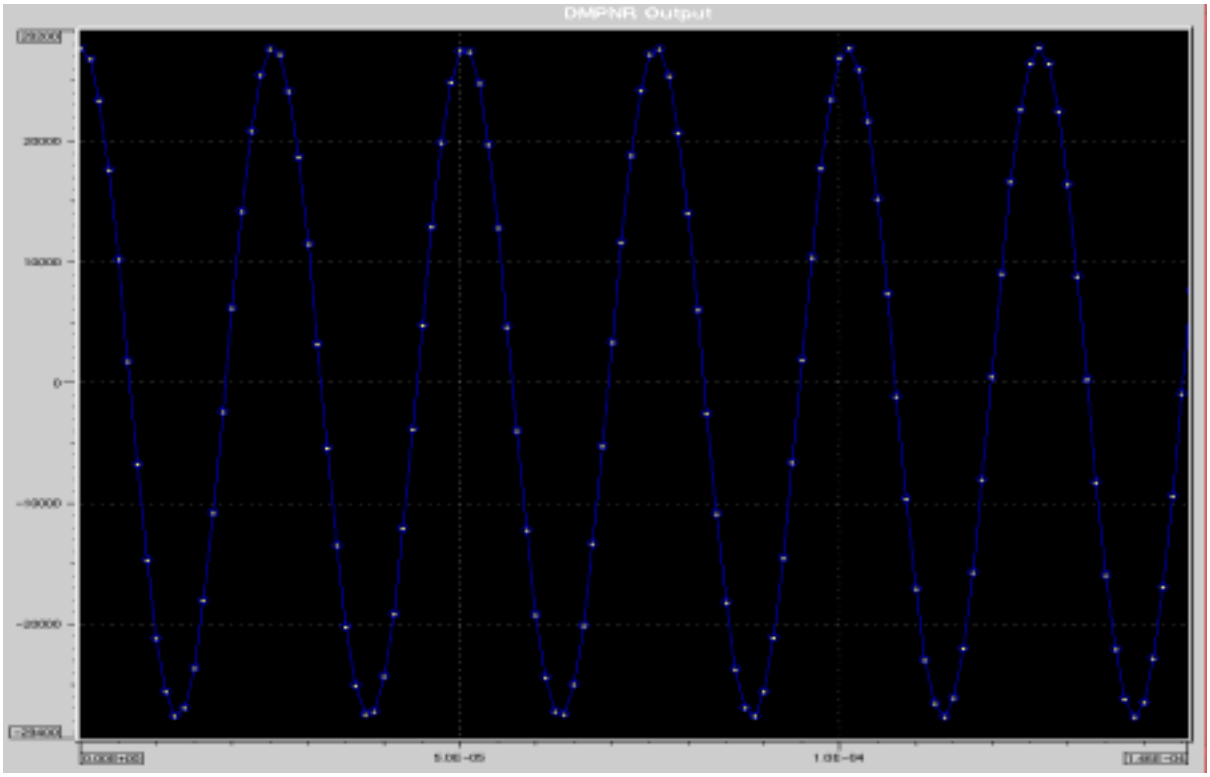

Fig. 7.4: The testing stimulus – digital sinusoidal waveform (SNDR=96.15 dB)

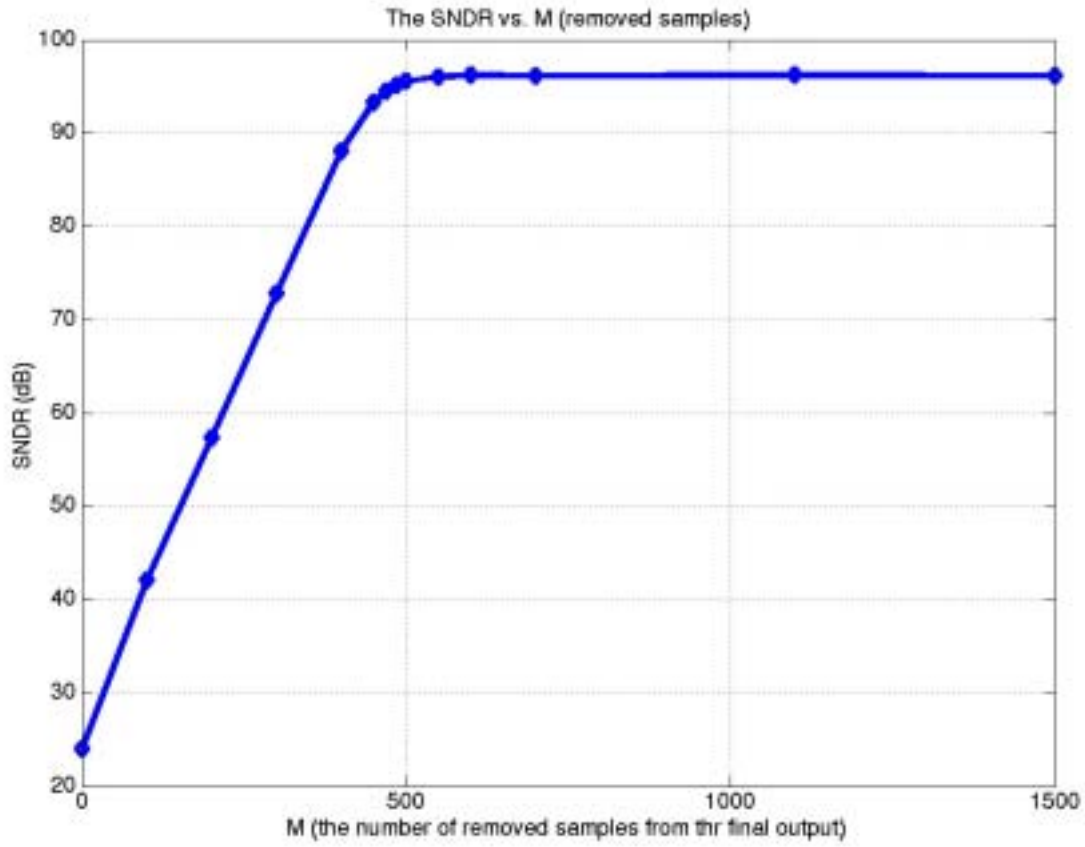

Fig. 7.5: The SNDR values with different *M* samples

Table 7.2: The SNDR values with different *M* samples

M	0	100	200	300	400	450	470
SNDR(dB)	23.93	42.10	57.30	72.85	88.10	93.30	94.41
M	485	500	550	600	700	1100	1500
SNDR(dB)	95.13	95.55	96.05	96.19	96.18	96.20	96.17

From Fig. 7.5 and Table 7.2 the SNDR is continuously improved with the increasing value of M. And this improvement will not be accelerated any more when M is bigger than 500. So we fix M to 500 in the design. Then the transfer character of the notch filter is simulated. The simulation result is given in Fig. 7.6, where a notch peak at normalized frequency of 0.19 can be noticed, which means that the physical notch frequency is $0.19 f_s = 0.19 \times 8\ kHz = 1.52\ kHz$. It is exactly the testing frequency produced through the on-chip signal generator and, of course, the output signal from the loop structure. After the calculation the attenuation at the notch frequency of this filter is above 100 dB, which means that the signal of the interest can be removed from the output signal of the loop effectively. At last, the simulation for the total Loop BIST is performed and the BIST result is compared with the theory value (design specification) in Table 7.3, which gives the demonstration of the Loop BIST approach.

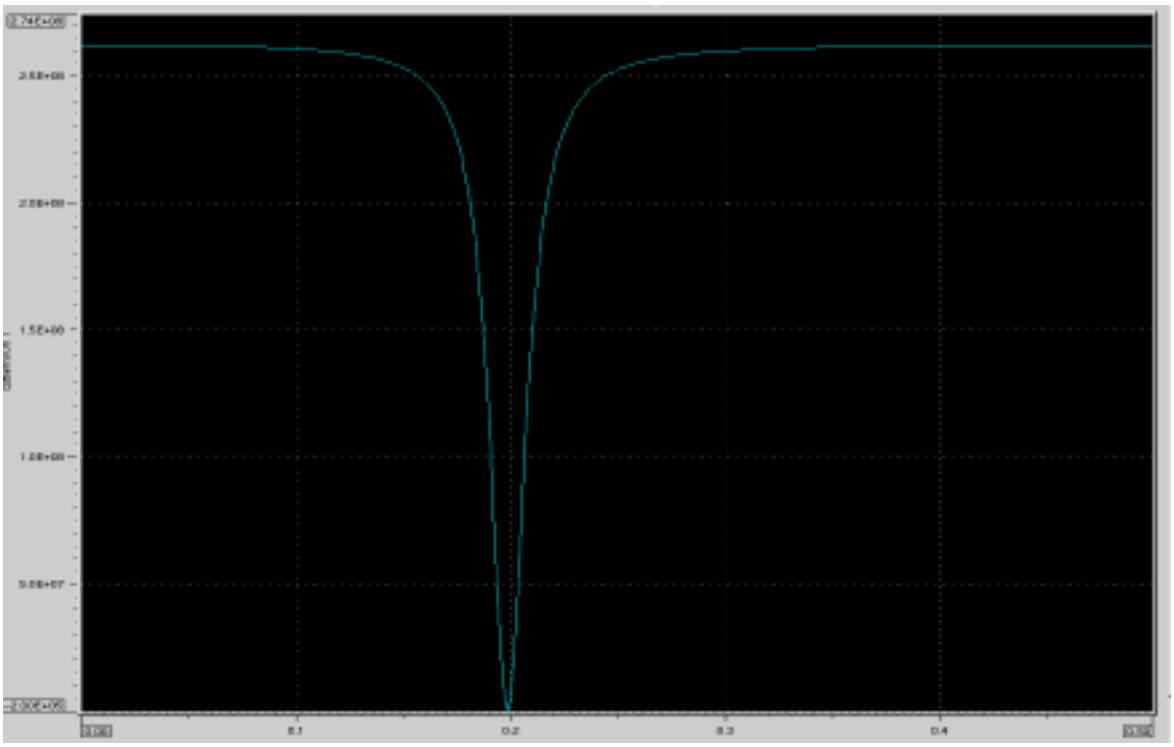

Fig. 7.6: Characteristic of the notch filter

Table 7.3: Loop-BIST result

	SNDR (dB)
Theory value (design specification)	96 dB
BIST result	95.5 dB

7.3 Implementation of Loop-BIST for C2 (Case 2)

7.3.1 Circuit under Test (CUT)

In this case, the circuit under test is similar to that in Chapter 7.2. It is still a voice-band code part in a GSM front end chip. The chip is illustrated in Fig. 7.7 and the voice band path is located in a rectangle with light dashed line. In fact, the chip in this case (C2) is very similar to that in Chapter 7.2 (C1). The difference between these two chips is that in the voice band part of C2 the SNR of the ADC in transmitting link is only 70 dB, which is smaller than that of the DAC (90 dB) in the receiving link on the same chip. Meanwhile, all the other components have the same performances as those in C1. The block scheme of the Circuit under Test (CUT) is illustrated in Fig. 7.8.

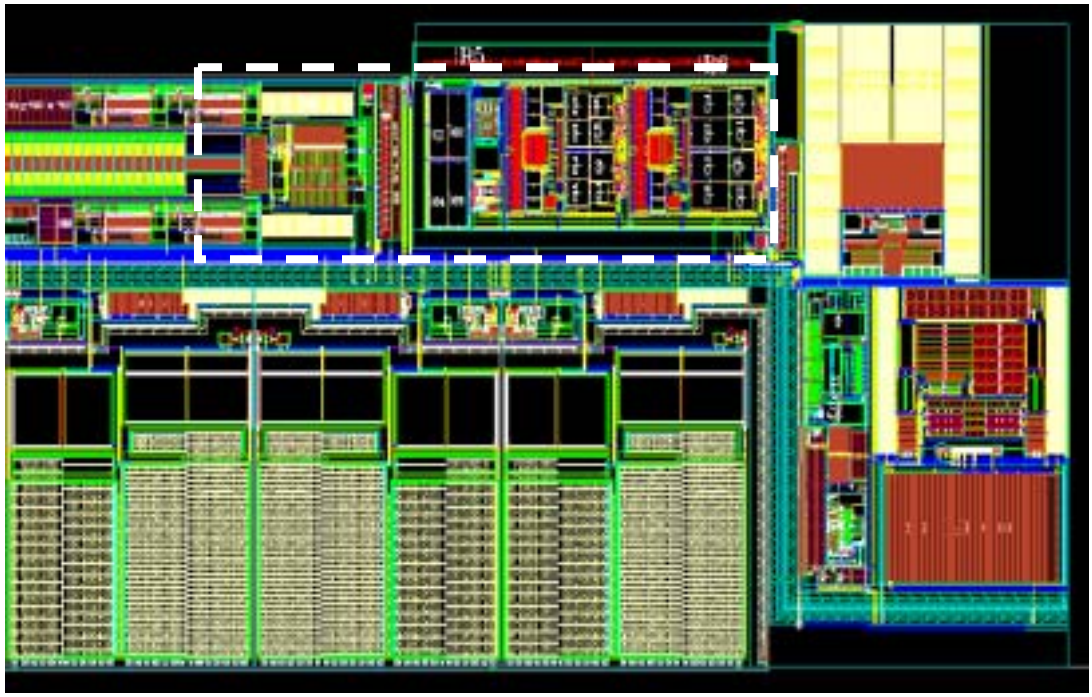

Fig. 7.7: The Circuit under Test (CUT)

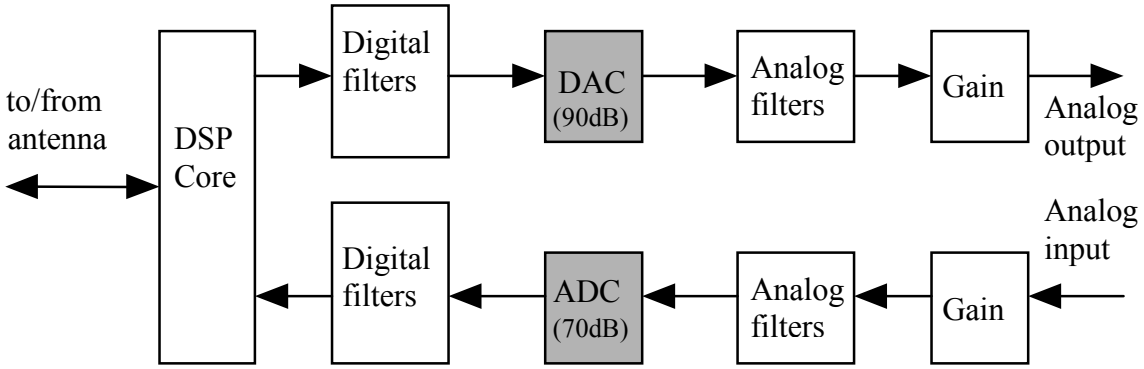

Fig. 7.8: Block scheme of the Circuit under Test (CUT)

The path to the earpiece contains digital interpolation filters, a digital-to-analog converter (DAC) and analog post filters. The DAC operates at a fixed frequency of 4MHz with a SNR equal to 90 dB. Meanwhile, the path from the microphone consists of an analog anti aliasing filter, an analog-to-digital converter (ADC) and digital decimation filters. The analog signal is over-sampled by a 2MHz ADC with a SNR of 70 dB, which is smaller than that of the DAC (90 dB) as well as that of the ADC in Chip A (90 dB). The multi-rate filters for both interpolation and decimation are also implemented on ASMD, specifically designed to run the WDF.

7.3.2 Loop BIST structure

Since the ADC branch meets a performance of SNR = 70 dB whereas in the DAC branch SNR = 90 dB, the verification must be carried out first in the branch with lowest yields. Otherwise, the branch with lowest performance (ADC branch) would degrade the signal to a point below the performance of DAC branch and this branch could be never verified by the Loop-BIST. Therefore, a DAC-BIST is very essential for the Loop-BIST in this case. The structure and algorithm are present in Chapter 3.3.2 and Fig. 3.6, respectively. Thus the Loop-BIST process is 1) DAC-BIST 2) Loop test; the last step (Loop test) is identical to the testing process in Chapter 7.2. So in the next section, a new BIST method for the DAC SNR testing will be introduced.

7.3.3 A new BIST method for DAC SNR testing

The goal of the DAC-BIST is the SNR testing of a DAC in the range of speech processing (sampling rate 4MHz, testing signal frequency 1.5 kHz), without using memory units on chip. In Chapter 2.4, lots of BIST methods for the testing of mixed-signal

components have been introduced. These methods either are designed for ADC BIST ([43] [44]) or need on-chip RAM ([37] [45] [61]) or require a long testing time [81]. Considering the various shortcomings of these BIST methods, a new DAC BIST method for the SNR testing is then designed, in which a new one-point-one-comparison algorithm is employed, comparing the desired signal by each tracked point with a rising reference voltage with a comparator, instead of the multi-comparison in [81].

7.3.3.1. DAC - BIST architecture

Fig. 7.9 shows the block diagram of the components comprising the proposed on-chip DAC BIST structure. It consists of a digital sinusoidal wave generator that produces a 1.5 kHz digital sinusoidal waveform as the testing pattern, a periodic waveform digitizer, and a notch filter reserving as the digital-processing unit to extract the SNR of the input from the digitizer. All of the components are synchronized by a clock tree and controlled by the testing control logic. The output of the notch filter will be transmitted into the testing control logic to be compared with the expected one. The test is passed if the obtained result falls within acceptable ranges, otherwise it is failed. The on-chip digital sinusoidal signal generator and digital notch filter are reused, both described in Chapter 7.2, to generate the test pattern and to extract the SNR value of the signal. A description of the on-chip digitizer will be presented as follows.

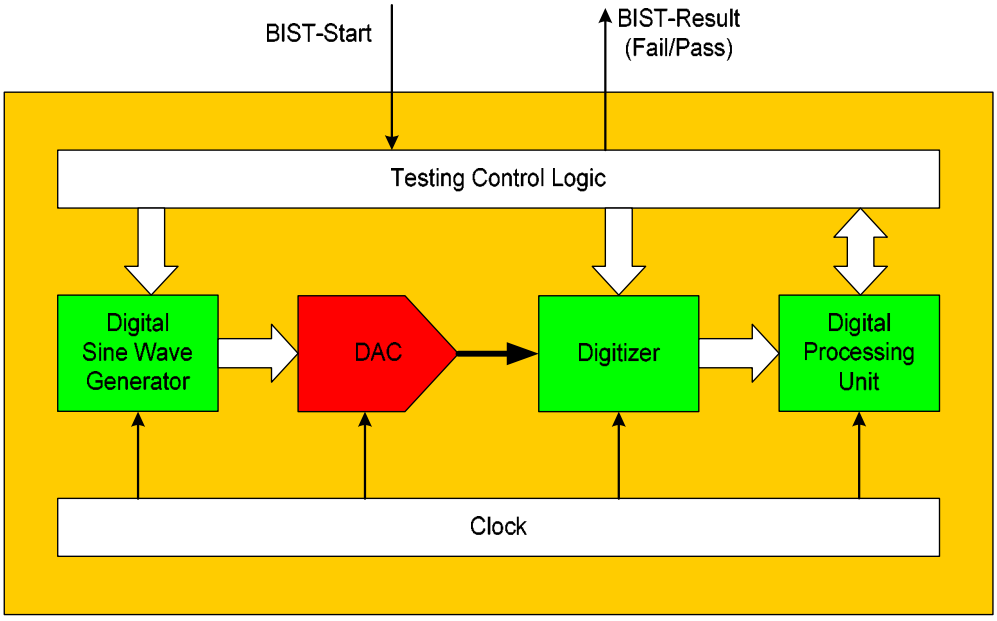

Fig. 7.9: Block diagram of the proposed BIST system

In [81], an on chip signal extractor is proposed. The principle of this approach is like that of an AD converter. This extractor can convert the periodical signal into its digital value, by exploiting the periodicity of analog signal under test and making multiple comparison passes over progressive periods of this signal. The extractor consists of a single comparator and a robust on chip reference voltage generator. Sub-sampling technique is used to enable the capture of analog waveforms using a single comparator clocked appropriately (Fig. 7.10).

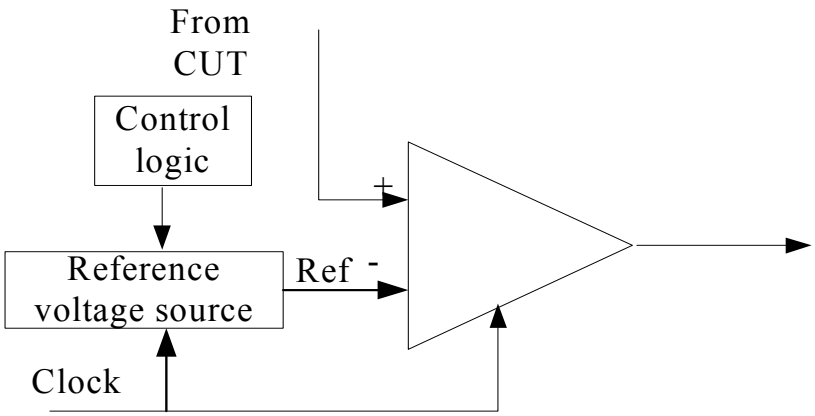

Fig. 7.10: On-chip digitizer [81]

Arbitrary amplitude resolutions are achieved by varying the reference comparison level input to the comparator (Vref), which is held constant for the duration equal to the time it takes the comparator to compare all samples of the UTP (Unit Testing Period) to this reference level. Once all comparisons are made, Vref is incremented to the next quantization level and the process is repeated. At last, the passed number of each sample is then its digital value, thus we can get a digital signal through such a comparison method. It is obvious that the quantization level determines the resolution of this on-chip digitizer. Since it compares all the samples with the same level within the same quantization level, this method is called as Multi-Point-One-Level (MPOL) comparison method. However, the DAC on this chip works in the speech processing range. Thus the testing stimulus should be a sinusoidal wave with a 1.5 kHz frequency. For a 16-bits DAC (since SNR = 90 dB), the BIST solution should have at least 18 bits resolution (2-3 bits more than CUT), which means the multi-comparison algorithm needs $(2^{18}/1.5)$ ms = 175s, about 3 minutes for a whole testing. That is too long for the production testing and some adaptation must be made to this on-chip digitizer. Since, ny CMOS technology, a design with a sampling rate of ten million HZ is not big problem today, it is possible to compare each point with all the reference stages and then deal with the next point, thus a much shorter testing duration can be achieved. The block

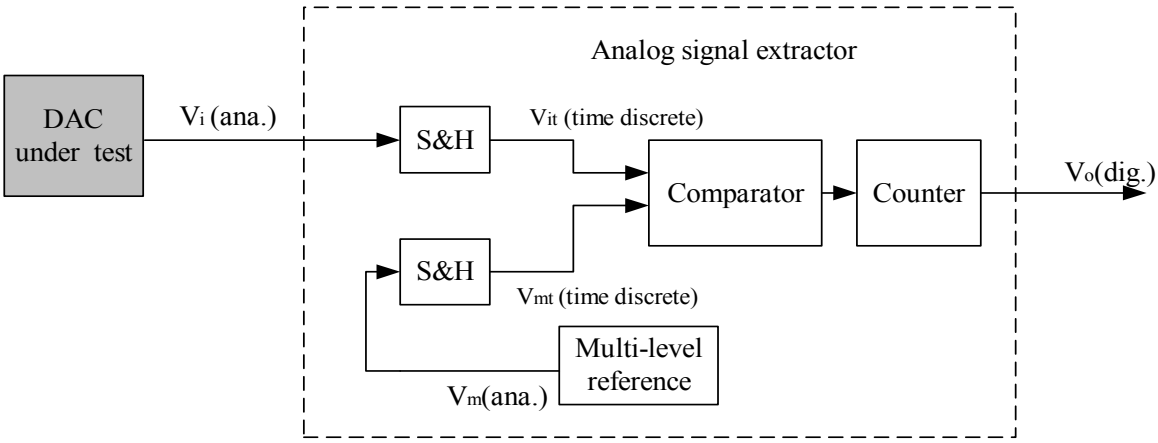

Fig. 7.11: On-chip signal extractor

scheme is illustrated in Fig. 7.11. The analog output V_i from the DAC under test is sampled by a sampling-and-hold circuit (S&H) into the time discrete signal V_{it}, and the analog output of the multi-level reference voltage V_m is sampled by an identical S&H into V_{imt}, then V_{imt} and V_{it} are compared and the passed number is calculated in a counter. The two S&H's should be designed in the same structure and should be placed as near as possible by layout, so that the offsets of these two S&H's are identical and have no influence on the final comparison result [81]. The comparison process is shown in Fig. 7.12.

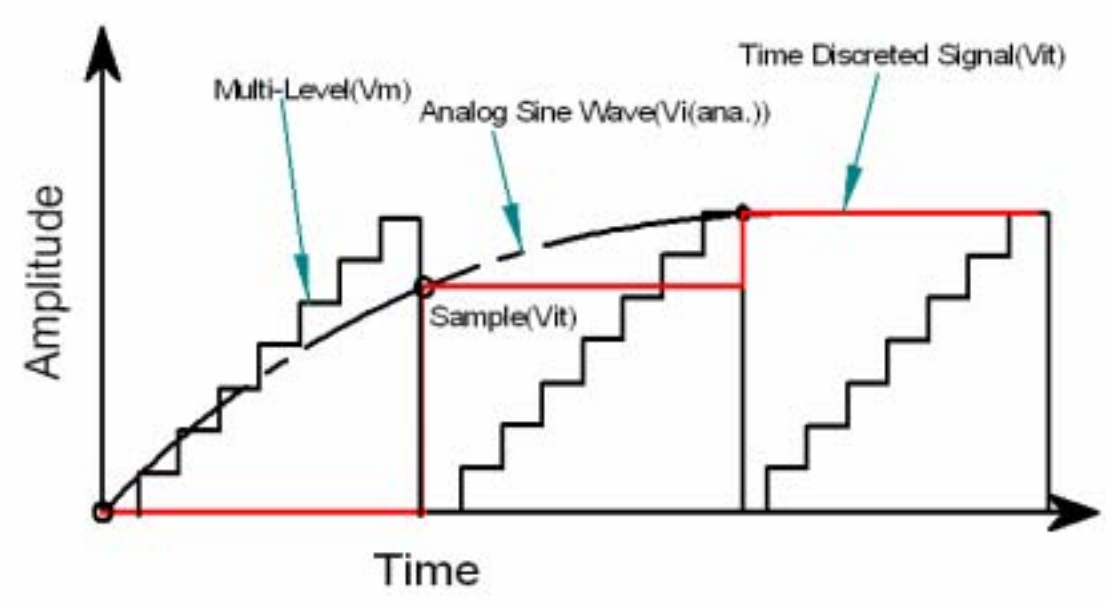

Fig. 7.12: One-point-multi-level comparison

Time discrete signal V_{it} is compared with V_{imt} in one sample duration and the passed

level is then the digital value of this sample point. Such comparison is repeated in the next sample duration till the last sample. Finally, a digital signal can be outputted after the on-chip digitizer. A further strategy to decrease the testing time is the usage of two-step comparison method. It minimizes the comparison steps in order to reduce the total testing time. The two-step comparison technique is derived from ADC technique. During AD conversion, the two steps AD conversion technique is usually used when the resolution requirement is too small. This two-steps architecture consists of a sampling-and-hold circuit, a coarse flash ADC, an analog substractor, a fine ADC, a DAC stage and a digital bits-combiner. During two-step testing, first the S&H tracks the analog input and holds it for the coarse conversion and subtraction operation. Then the coarse flash ADC makes a coarse digital estimate of the analog input (discrete-time signal) to yield a small voltage range around the input level. The DAC stage converts this digital estimate into an analog signal, which is deducted from the original analog signal through the substractor. The fine ADC subsequently digitizes the residual signal. Lastly, the digital outputs of the coarse ADC and fine ADC are combined to the final output. Setting the resolution of the coarse ADC and the fine ADC properly (for instance, in this case, each has a resolution of 9 bits), the on-chip digitizer can be reused both for the coarse and fine AD conversions, which leads to a much simplified structure of the two step comparison as illustrated in Fig. 7.13.

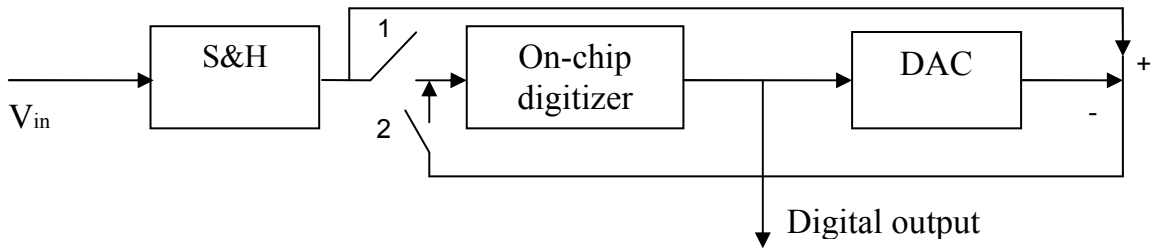

Fig. 7.13: Two step comparison

The usage of coherent-sampling technique [83] provides a possibility that all the sampled points are sampled with several periods but not in one period which relaxes the design of the S&H and the comparator. The design of the reference voltage generator in Fig. 7.11 is based on the delta sigma modulation described in Chapter 5.5. A software delta-sigma modulator converts the desired signal into a 1-bit stream. Then this bit stream is transmitted into a 1-bit DAC that is followed by an analog low pass filter. The low pass filter removes the out-of-band high-frequency modulation noise and therefore restores the original waveform. By implementation a set of points from the bit stream is extracted. This bit stream contains an integer number of signal periods in terms of some criteria, since the bit stream of a periodic signal is not even a periodic

one. Then these points are stored in the on-chip memory, which is applied to the 1-bit DAC and the low-pass filter periodically to generate the desired signal.

7.3.3.2 Simulation results with MATLAB

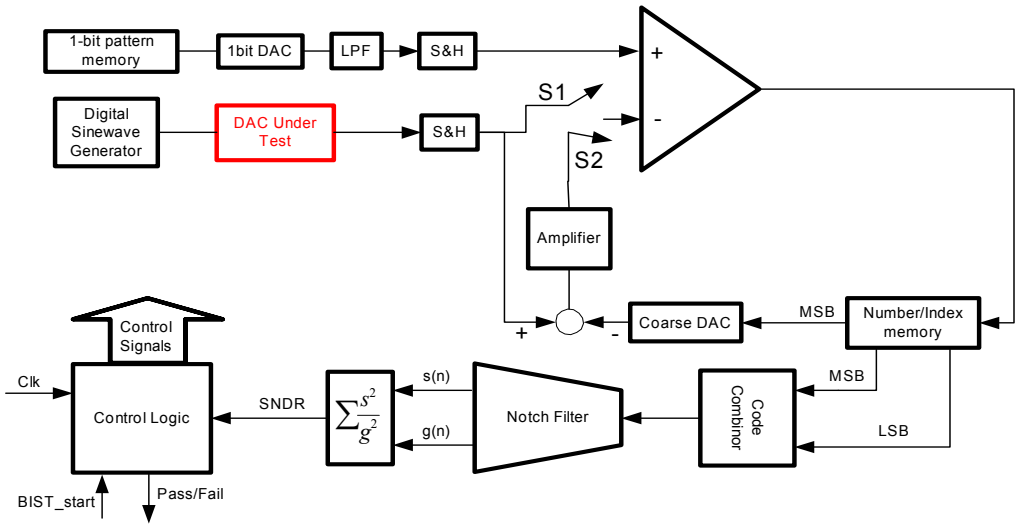

Fig. 7.14: DAC BIST scheme

To verify the correctness of the design, the system is modeled and simulated in the MATLAB environment. The overall BIST topology for the proposed DAC BIST scheme is depicted in Fig. 7.14. The required functional blocks and control signals are described in the following:

- *bit pattern memory, 1-bit DAC and LPF* together produce the reference voltage, which rises from –1.85 V to +1.85 V with 2^9 small stages and each stage lasts UTP/2^9 with a UTP (Unit Test Period) = 25.6 μs.

- *The digital sinusoidal wave generator* generates a digital sinusoidal stimulus using the method we have introduced above. The system parameters are available in Table 7.1.

- *The two S&H's* before the comparator resample the signal with coherent sampling technique [83] so that the DAC output will hold constant while the reference voltage rises through the full scale, which is different with the

other method [81]. The reason is that the CUT is a codec chip, whose testing signal is typically 1.5 kHz.

- *The notch filter and the SNDR meter* are the signal evaluation systems.
- *The control logic* controls the BIST processing and gives the final BIST result.
- *The comparator, the code/index memory, the coarse DAC, the amplifier and the substractor* build up a two step conversion unit.
- *Switches S1 and S2* control the comparison step. For a coarser comparison, S1 close and S2 open; while for a fine comparison, S2 close and S1 open.

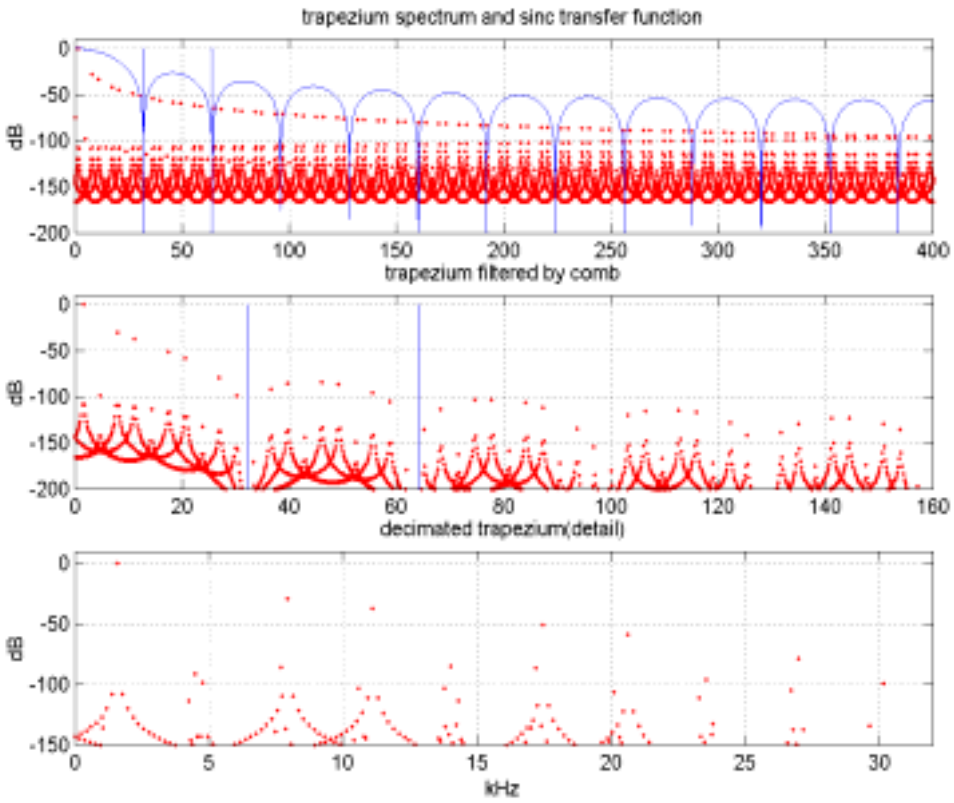

Fig. 7.15: (a) spectra of input signal with decimation filter; (b) decimation filter output; (c) decimated signal with aliased frequencies

For the simulation of the testing stimulus, the following parameters are set: f_s = 800 kHz, n = 14, INC = 65 and f_0 = 1.5869 kHz. By simulation, 98304 sample points are collected. The anti-aliasing filter is a 2nd order sinc-filter. The spectra at different

phases are shown in Fig. 7.15. In Fig. 7.15(a) the in-band frequencies due to INC = 65 are visible. The notch in the sinc filter's magnitude identifies the central position of the aliased spectra which the decimator with a factor DEC = 25 produces. At this frequency the signal's components are too strong and the use of a filter is mandatory. The notch filter is modeled as a band-stop filter described in Chapter 6.5 with $a_1 = -0.3188$ and $a_2 = 0.8825$. The notch frequency is 1.5 kHz and sampling rate is 8 kHz. A Gaussian noise with $\delta = 1$ and a noise level of 0.17783 mV is added to the filter input. The output of the notch filter consists of the noise and the distortion, and the estimated signal is obtained by removing the notch output from the original input. Fig. 7.16 shows the estimated value and real value of signal and noise, respectively. Fig. 7.16(a) and (c) show the estimated value of signal and noise, and Fig. 7.16(b) and (d) show the real value. Owing to the large simulation samples, only 100 points of them are shown. From the simulation we can see that the matching errors between the estimation and real values are very small.

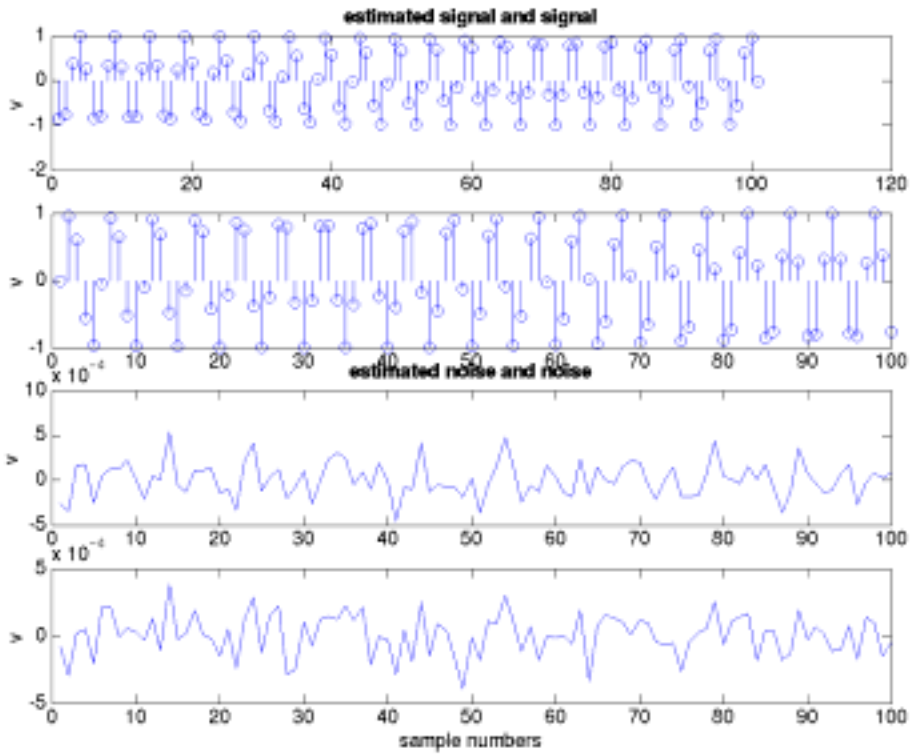

Fig. 7.16: Estimation results of the notch filter

To validate the proposed digitized technique, we perform numerical simulation by applying the sinusoidal signal to DAC under test. The CUT is modeled as a 16 bit DAC with the full scale voltage of 3.7 V. The simulation results are shown in Fig. 7.17, which shows that the performance of this DAC BIST method can achieve 120 dB. Of

course, this is enough for our case whose DAC is only 90 dB.
It should be noted that the design of on-chip digitizer belongs to the domain of analog circuit design, which has been discussed in detail in [81]. But with respect to the total design efforts, the analog design is always more difficult and thus should be spent more efforts than the digital design. So the design of a DAC BIST is still more complex than the design of an ADC BIST, in spite of the simple structure of the DAC BIST as described above.

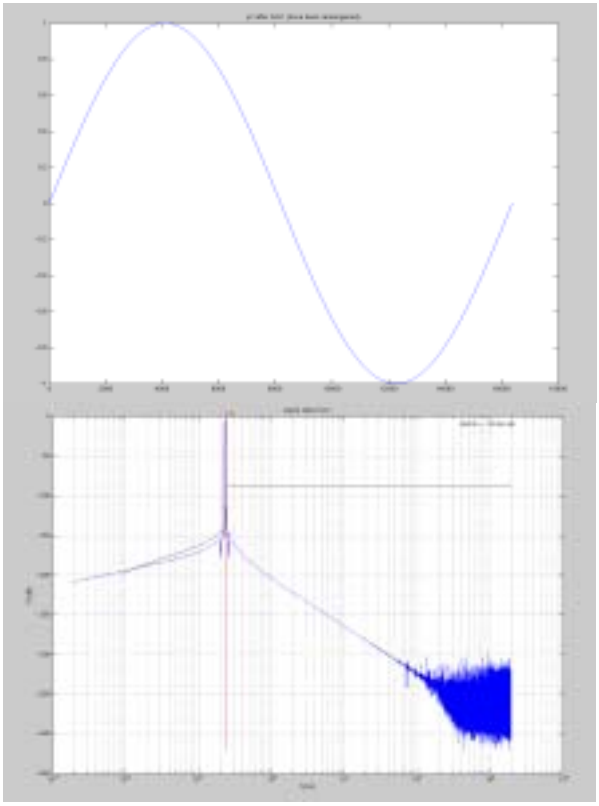

Fig 7.17 (a): Sinusoidal waveform after the on-chip generator

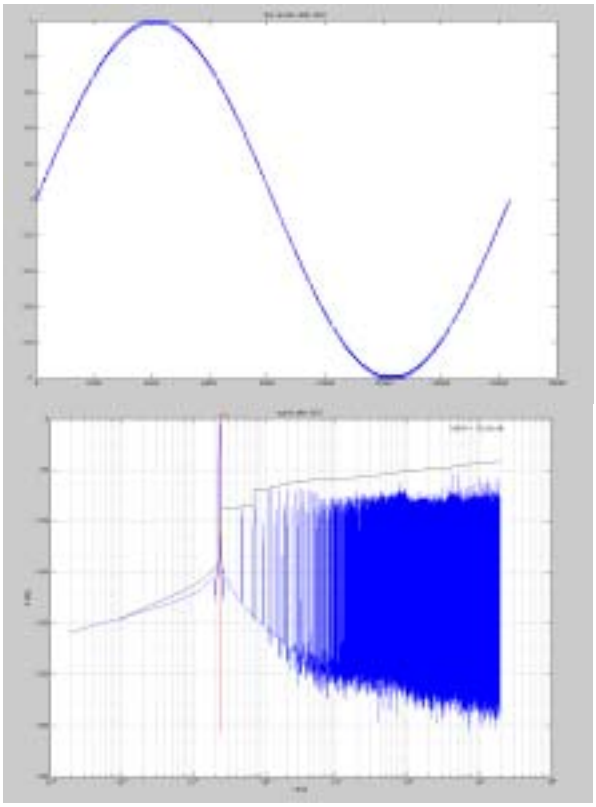

Fig 7.17(b): Digitized signal for DAC output.

7.4 Implementation of Loop-BIST for C3 (Case 3)

7.4.1 Circuit under Test (CUT)

The circuit under test is a mixed signal front-end of a dual-mode base band processor on an IEEE 802.11-series compliant dual-band WLAN (Wireless Local Access Network) chipset. The Circuit under Test (CUT) is the Analog Front-End (AFE) macro of this WLAN chip, whose block scheme is illustrated in Fig. 7.18.

The AFE covers the IEEE802.11a and IEEE802.11b standards, which means that the block operates in two different modes: in IEEE802.11a-mode the ADCs operate at 80 Msps and their resolution is 10 bits, while the DACs operate at 80 Msps and their resolution is 9 bits; in IEEE802.11b-mode both the ADCs and DACs operate at 44 Msps with a resolution of 7 bits.

The ADCs convert the differential RX_I and RX_Q signals from the analog to the digital domain. In IEEE802.11a-Mode the RF-signal is down-converted to a low Intermediate Frequency (IF) with a centre f_m = 10 MHz. In IEEE802.11b-Mode the RF-signal is down-converted to Zero-IF. The DACs convert the TX_I and TX_Q signals from the digital to the analog domain. A 2nd order Butterworth filter reduces out-of-band-energy, which is also served as a reconstruction filter. In IEEE802.11a-Mode the base band signal is up-converted in the RF-Chip from Zero-IF or from Low-IF with a centre frequency f_m = 10 MHz. Both transmission-modes are supported. In IEEE802.11b-mode the base band signal is up-converted in the RF-Chip from Zero-IF.

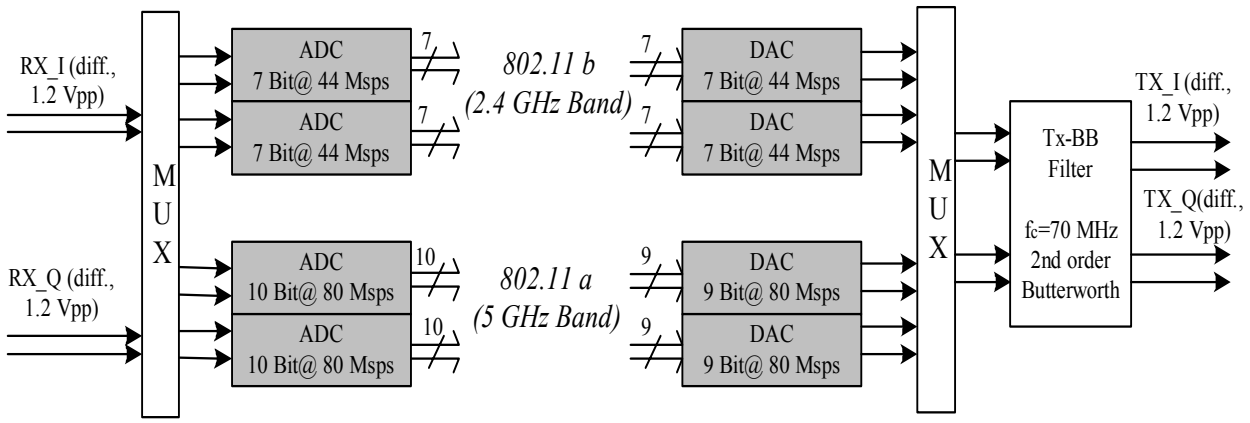

Fig. 7.18: Block scheme of the CUT

7.4.2 Loop BIST structure

In IEEE802.11b-Mode the DACs and ADCs operate with the same resolution of 7 bits. The approach in Chapter 7.2 can be adopted and reused for the testing in this mode, which will not be discussed further. However, in IEEE802.11a-Mode the ADC branch meets a performance of 10 bits resolution whereas in the DAC branch the resolution is 9 bits, which means that the verification must be carried out first in the branch with lowest yields. Otherwise, the branch with lowest performance (DAC branch) would degrade the signal to a point below the performance of ADC branch and this branch could be never verified by the Loop-BIST. Therefore, in contrast to Chapter 7.3, an

ADC-BIST must be carried out at first in this case. The structure and algorithm are available in Chapter 3.3.1 and Fig. 3.4. Thus the Loop-BIST process is 1) ADC-BIST 2) Loop test; the last step (loop test) is identical to the testing process in Chapter 7.2. So in the next section, the ADC BIST method for the Loop-BIST testing will be introduced.

7.4.3 ADC BIST

BIST for ADC requires both generating analog test stimulus and evaluating digital test responses on-chip. Both of them should be implemented by making use of the existing circuitry and adding some additional hardware on-chip. But the hardware overhead should be kept to a minimum by reconfiguring. In Section 6.5 and Section 7.2, an approach to extract the SNR of a digital signal through a notch filter has been introduced and implemented respectively. Now the difficulty in the test is to generate an analog testing stimulus. There are mainly two ways to test an ADC: the static test by using a ramp stimulus to make a histogram test and the dynamic test in the frequency domain by using a sinusoid stimulus. There are practically several disadvantages by using a ramp stimulus. Firstly, a histogram test for an ADC static test often needs to capture all the samples 8-16 times so as to remove the random noise by averaging, which means the total testing time is too long, especially for high resolution ADC. Secondly, due to the rise, fall and settling time at each step, a ramp stimulus is more difficult to be generated precisely than a sinusoidal signal [84]. The fact that the input ramp must have at least two more bits of the resolution than the ADC being tested makes it more difficult for high resolution to generate a precise ramp signal as the testing stimulus. An analog sinusoidal wave with SNR above 75 dB is selected as the testing stimulus in this work. In fact, a pure sinusoidal waveform is easy to generate with a DELTA-SIGMA modulator and a LPF (Low Pass Filter), which was described in Section 5.5. Then the frequency response and SNDR value of the ADC can be obtained by using a digital notch filter or through FFT calculation in a DSP (Digital Signal Processor). The block scheme of the suggested ADC BIST is illustrated in Fig. 7.19.

As described in Section 5.5, the sinusoidal waveform signal is generated by using a digital method with high precision at low hardware complexity. First of all, a sinusoidal waveform is converted into a bit-stream by a DELTA-SIGMA modulator, which is carried out in software. Thus there is no limitation by stability and order for the DELTA-SIGMA modulator. Secondly an *N*-point portion is selected from this bit-stream with some chosen condition [39] [40]. Thirdly, this *N*-point portion is stored

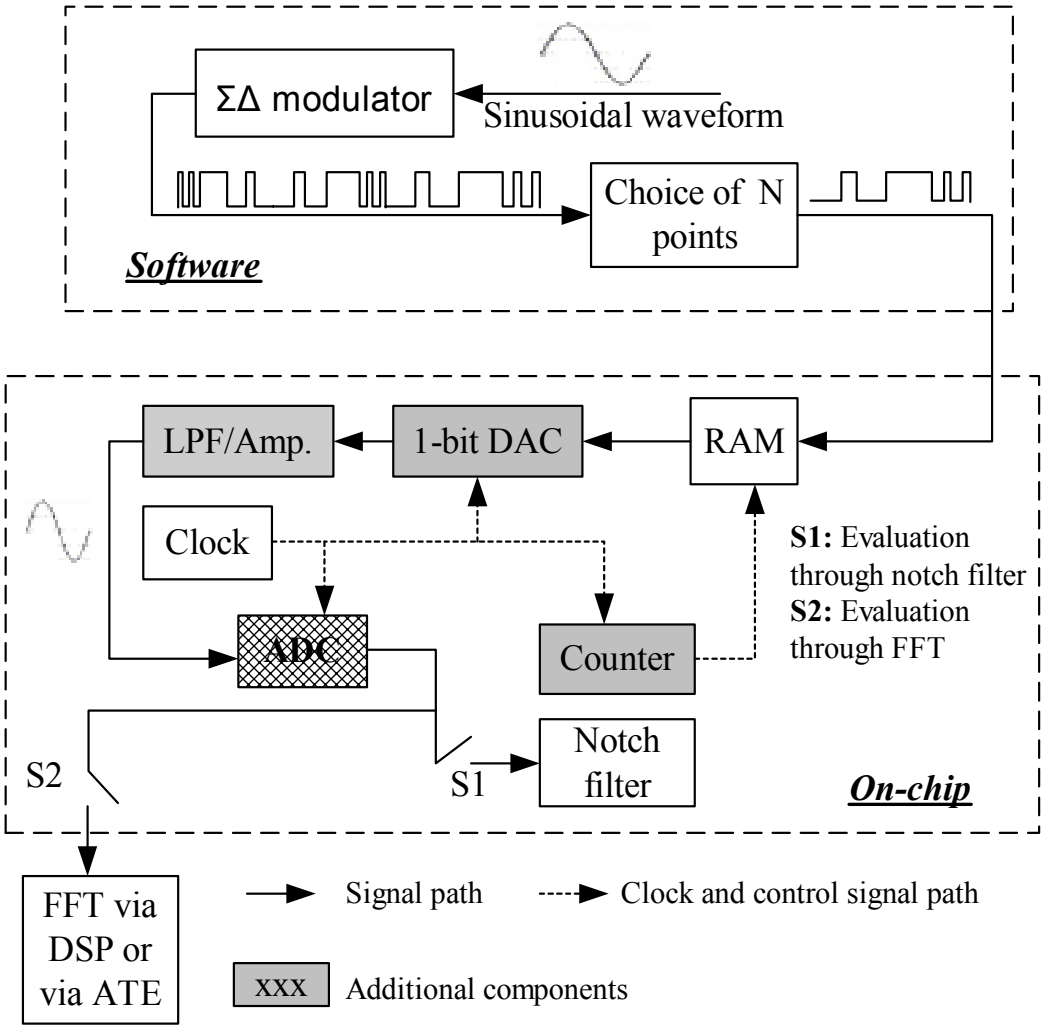

Fig. 7.19: ADC BIST

on-chip in the memory or in a register chain consisting of *N* flip-flops. During the test, the bit-stream is repeatedly read out by a clock with proper frequency and then filtered through an analog LPF. At last, a pure sinusoidal signal as the testing stimulus can be obtained because the bit-stream to approximate the bit-stream has a very low noise level at a low frequency. The digital output of the ADC can be directly captured by the notch filter to extract the SNR. For the notch filter, we can reuse the design in Section 7.3. Then the additional hardware is a simple LPF, a 1-bit DAC and an index counter for the RAM. The design of the counter belongs to the digital domain. The 1-bit DAC makes the transition from the digital codes (logic '1' and logic '0', namely digital V_{dd} and V_{ss}) to analog domain (analog V_{dd} and analog V_{ss}). It acts as a buffer between the digital logic to analog filter. This 1-bit DAC needs to work at the same speed as the index counter.

Now let us discuss the design of analog low pass filter. As mentioned earlier, the bit-

stream is noise shaped, with noise at the high frequency band so that the in-band noise is even less. The analog output of the 1-bit DAC still has the same noise shaping character as the bit-stream, which needs, therefore, to be filtered by an analog low pass filter, so that the high frequency noise can be removed to obtain a high quality analog signal.

The choice of the analog low pass filter is guided by the chosen NTF (noise transfer function) of the DELTA-SIGMA modulator and the attenuation of the out-of-band noise needed. Fig. 7.20 shows the noise shaping characteristic of the 5^{th} order vs. the 2^{nd} order modulators. From this figure, we can see that the higher order modulator has the lower in-band noise that leads to a higher SNR value, but the higher order modulator has also the higher out-of-band noise which needs higher order Low Pass Filter (LPF) to attenuate out-of-band noise of the modulator. According to [39] [40], the performance of the analog signal depends on the chosen analog LPF following the modulator. In general, the order of analog LPF should preferably be one order higher than the loop filter order of the delta sigma modulator to suppress the high-frequency noise. Otherwise, the analog signal generated will be affected by the nonlinearity of the LPF.

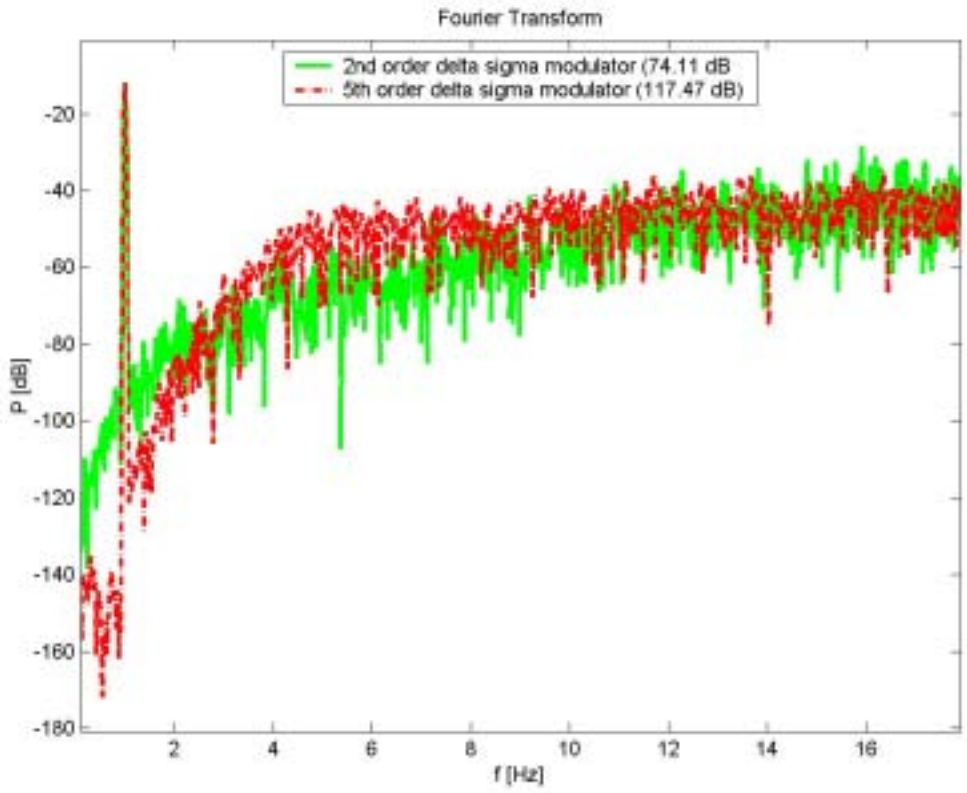

Fig. 7.20: 2^{nd} order vs. 5^{th} order modulator frequency response

The goal is to test a 10 bit ADC. An analog signal with 12 bit accuracy is needed for the test. Considering the random noise in the 1 bit DAC and the analog LPF that fur-

ther deteriorate the signal's quality, 13 bit accuracy signal is needed from the modulator that is generated in software. A 5th order modulator introduced in Section 5.5.1.4 is employed, which can achieve 13 bit accuracy with an OSR (Over Sampling Rate) = 7. This relaxes the design of clock for repeatedly sending out the stored the bit-stream on chip. Thus, a 6th order Butterworth LPF is designed to eliminated the out-band noise of the bit stream. The LPF scheme is given in Fig. 7.21. The design for the element parameters of the filter can be found in [74] [75] and we will not discuss them in detail. The circuit has four stages of operational amplifiers. The first three stages are applied for the filtering, the last one is used to amplify the output voltage and as well as to adjust the DC level of the output to the required range for the ADC being tested.

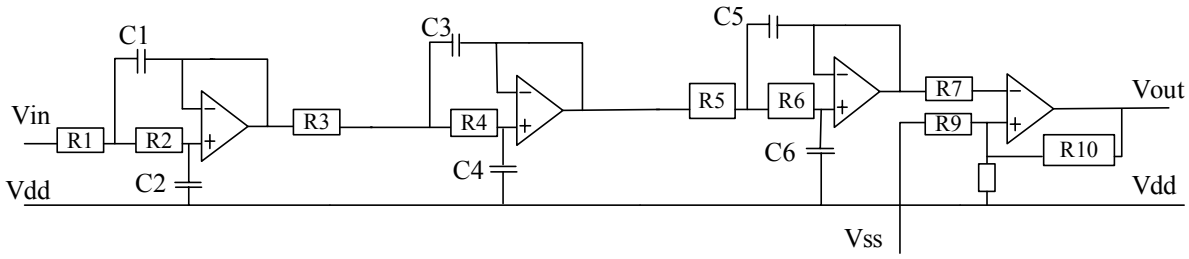

Fig. 7.21: Design of 6th Butterworth LPF

For a practical system, the Low Pass Filter (LPF) can reside off or on chip. As shown in Fig. 7.22, a LPF is designed off-chip, which gives many merits for calibration and characterization [76]:

1) it gives full flexibility in the pass band choice for extending the ranges of signals that can be generated;

2) the filter can be tuned to optimize its performance.

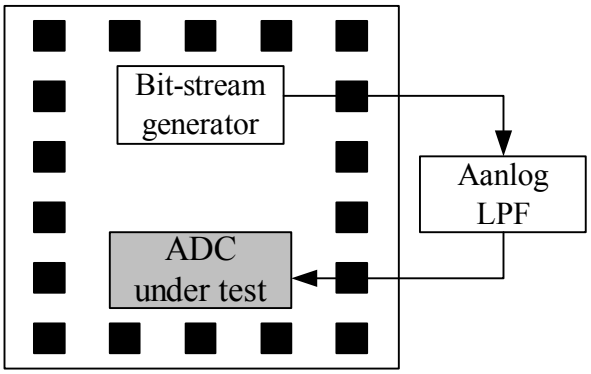

Fig. 7.22: Analog LPF off-chip

7.4.4 On the practical implementation of the ADC/DAC BIST

It should be noted that there are some RAM on this WLAN chip, which gives more flexibility for the design of BIST. In Section 7.4.3, memory on-chip is reused to store a N-point portion from the bit-stream output of the DELTA-SIGMA modulator so that it can be repeatedly read out for approximating a sinusoidal waveform signal. In fact, a very simple approach was introduced in Section 6.1, making use of the RAM/ROM on chip to generate a digital sinusoidal waveform as the testing stimulus. An analog testing stimulus for other analog parts on chip can be obtained by setting a DAC after the RAM. A practical way to test the ADC is to combine RAM with DAC to form an analog testing stimulus generator. But the problem by such combination is that the resolution of the DAC on this WLAN chip is less than that of the ADC on the same chip. This would degrade the analog testing stimulus after the DAC so that it is not suitable to test the ADC any more. One trick to fix this problem is to place an analog Band Pass Filter (BPF) after the DAC in order to improve the performance of the analog testing signal as shown in Fig. 7.23.

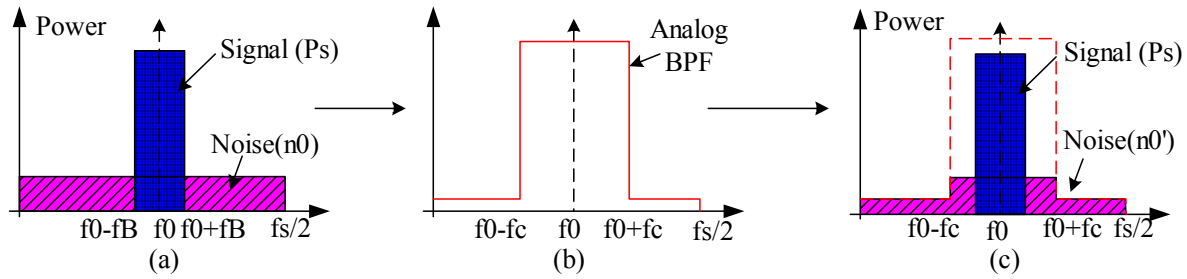

Fig. 7.23: Improvement of SNR through an analog band pass filter

Fig. 7.23(a) shows the Power Spectrum Density (PSD) of a signal whose central frequency is f_0, the bandwidth is $2f_B$ and the power is denoted by P_s. When the sampling rate is f_s and the noise level inside the Nyquist frequency band is n_0 , the Signal-to-Noise Ratio (SNR) is given by:

$$SNR = \frac{2P_s}{n_0 f_s} \tag{7.3}$$

After filtering through an analog BPF with a bandwidth equal to $2f_C$, with $f_C > f_B$ (the transfer characteristic is shown in Fig. 7.23(b)), the PSD of the signal is illustrated in Fig. 7.23(c). The noise out of the pass band of this BPF is greatly attenuated; therefore, the total noise power decreases as well. The final SNR is given by:

$$SNR = \frac{P_s}{2n_0 f_c + n_0^{'}(f_s/2 - 2f_c)} = \frac{2P_s}{4f_c(n_0 - n_0^{'}) + n_0^{'} f_s} \tag{7.4}$$

where $n_0^{'}$ is the new noise level out of the pass band after filtering. Since the resolution of the ADC is 1 bit higher than that of DAC on the WLAN chip, it is not so difficult to find a proper f_c and $n_0^{'}$ so that the analog signal after the DAC can be improved 3 bit (about 18 dB). After the verification, this ADC can be used to test the DAC with the Loop-BIST. The Loop-BIST scheme for WLAN chip is shown in Fig. 7.24. An analog BPF with 10.7 MHz central frequency and 100 kHz bandwidth (BW) is added between the DAC and the ADC to attenuate the noise and distortion out of its pass band and so as to improve the performance of the analog signal. By testing, switch 1 is closed and switch 2 is opened so that a loop consisting of Generation-RAM, DAC, analog BPF, ADC and Sample-RAM is formed. This is also the first loop. The testing pattern stored in the Generation-RAM has 1025 points (9-bits), covering ¼ of a period of a sinusoidal signal. The address is generated internally with increment one. The data from the Generation-RAM- is supplied to the DAC. The address is generated internally while the increment is taken from the JTAG register.

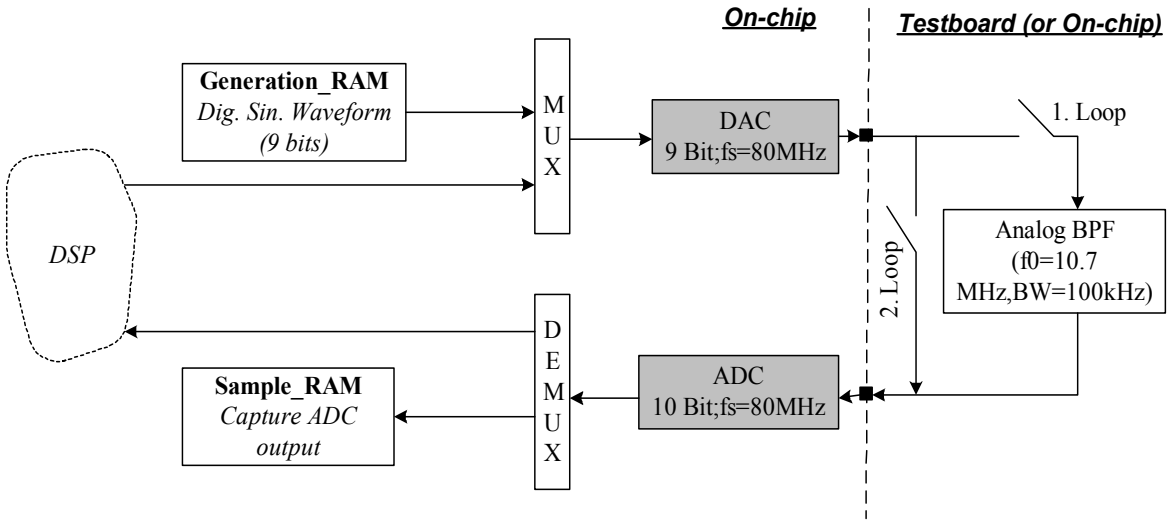

Fig. 7.24: Loop BIST scheme for WLAN chip

The analog signal from the DAC is filtered through the analog BPF, which can be implemented either on-chip or off-chip (e.g. on a load-board, see Fig. 7.22). By design, this analog BPF is implemented on a load-board because this can ensure to add the minimum additional hardware on the chip. The analog signal after the BPF has a higher resolution than the ADC to be tested. And the Sample-RAM captures 4096

samples from the output of the ADC under test. The data are transferred to the tester for analyzing.

After the ADC is verified, switch 1 is opened and switch 2 is closed to form the second loop without the analog BPF. In this way, the testing process is similar to that in the first loop. The only difference is that there is no BPF in the second loop and the ADC is already verified. Hence the second loop is able to measure and verify the DAC with the verified ADC.

7.5 Loop BIST for the DAC/ Delta-Sigma ADC pairs

The DAC BIST and the ADC BIST have been introduced in Section 7.3.3 and in Section 7.4.3 respectively. It can be seen clearly that an ADC-BIST would be much simpler and, thus, involve more digital design than a DAC-BIST. The ADC-BIST involves the generation of an analog testing stimulus and the evaluation of a digital signal, while the DAC-BIST involves mainly the generation of a digital testing stimulus and the evaluation of an analog response. Since the design of the analog parts dominates the total testing cost, it is reasonable to compare the design efforts of the analog components for the ADC-BIST and that for the DAC BIST. The design of a DAC BIST system needs several analog components; on the contrast, an ADC BIST needs only the implementation of an analog LPF, and this LPF can also be designed off-chip. Thus a cost-effective (simple and cheap) testing method can be achieved, if a DAC BIST could be converted into an ADC BIST under certain conditions. Furthermore, from Section 5.5.1 it is known that the SNR of a DELTA-SIGMA modulator can be changed with a different OSR. This is the basic idea of the testing method for verifying the DAC/ DELTA-SIGMA ADC pairs, which will be introduced as follows.

For instance, the DAC is a Resistor-string structure and its SNR is 85 dB. The ADC is a 2^{nd} order DELTA-SIGMA ADC with a SNR = 70 dB, which operates at 2 MHz (the highest permitted operating rate is 3.5 MHz). The cut-off frequency of the decimation filter after the modulator is 4 kHz. According to the testing specification the testing signal should be a 1 kHz sinusoidal signal. When applying loop BIST to this case, it is suggested that a DAC BIST be carried out first, because the performance of the DAC (85 dB) is much better than that of the ADC (70 dB). However, if the OSR of the modulator could be improved, a ‘new’ DELTA-SIGMA ADC would be obtained temporally, whose performance would be better than that of the DAC. This means that an ADC BIST could be applied first instead of a DAC BIST. In this way the goal is

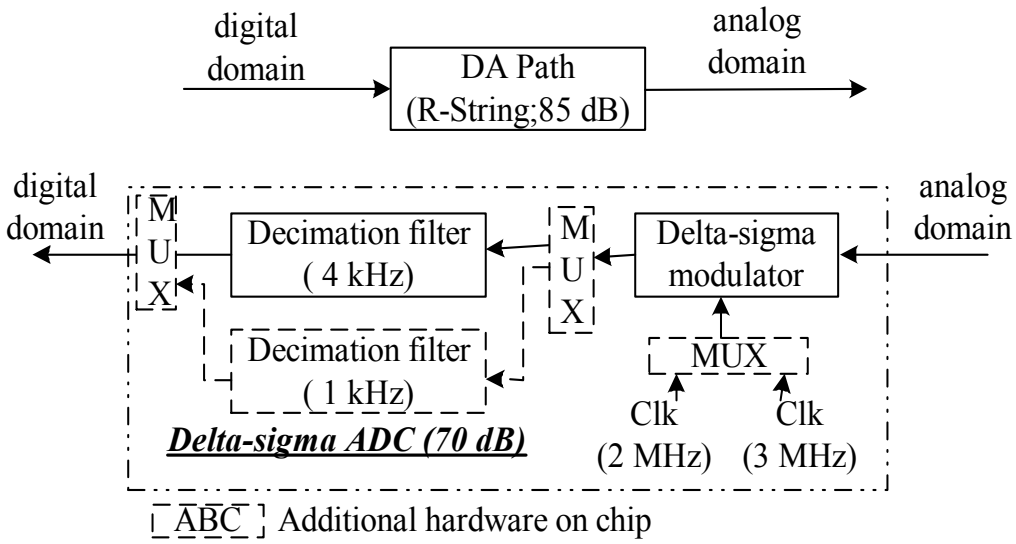

Fig. 7.25: Loop BIST scheme for DAC and DELTA-SIGMA ADC.

achieved. Fig. 7.25 shows the top level of the DAC/ DELTA-SIGMA ADC testing. The definition of the Over Sampling Ratio (OSR) is:

$$OSR = \frac{f_s}{2f_B} \tag{7.5}$$

where f_s is the sampling rate of the modulator and f_B is the cut-off frequency of the decimation filter. Hence there are two ways to improve the OSR of a DELTA-SIGMA ADC: 1) increasing the sampling rate; 2) decreasing the cut-off frequency of the decimation filter. The OSR in functional mode is OSR1 = 2 MHz/8 kHz = 250, which corresponds a DELTA-SIGMA ADC with a SNR = 70 dB. In BIST mode the sampling rate is set to 3 MHz and a new decimation filter is added; the new OSR is: OSR2= 3 MHz/2 kHz = 1500, which corresponds to a 'new' DELTA-SIGMA ADC with a SNR = 90 dB. Then the value of OSR for DELTA-SIGMA ADC can be increased so that the SNR of the modulator is improved and is higher than that of the DAC. Thus an ADC BIST can be applied instead of a DAC BIST, which leads to a cost-effective testing method. The Loop BIST for such a case has five sequential steps: 1) improving the OSR of DELTA-SIGMA ADC to get a higher SNR than that of the DAC; 2) executing ADC BIST; 3) testing DAC with this verified 'new' DELTA-SIGMA ADC (Loop BIST); 4) resetting DELTA-SIGMA ADC to normal working mode (decrease the OSR); 5) measuring the DELTA-SIGMA ADC with verified DAC (Loop-BIST). Finally, both ADC and DAC can be verified on chip. The limitation of this method is that there should be enough design margins in the DELTA-SIGMA modulator for improving the sampling rate; and the increase of sampling rate would lead to an unac-

ceptable addition of the power consumption. Furthermore, the additional overhead of the new decimation filter should be considered.

Since this method needs to change some components inside the CUT, it is preferred to say that this is a structure-based DFT approach. However, the method proposes a new way to get the trade-off between the design margins and the testing problem. Then the testing problem is transferred from the analog into the digital domain. Consequently, it leads to a cost-effective testing method in the industry production test.

Chapter 8

Conclusion and Future Work

In this dissertation a new approach for testing the analog components of mixed-signal chips has been proposed and examined. The aim is to design an easy and reliable testing method to test the ADC/DAC pairs. More importantly, it should be integrated on-chip to avoid the use of costly external tester equipments and ensure the portability in case of changes in technology. The improvements could be obtained by optimizing the proposed circuitry (for example, substituting the multiplier on the evaluation side with a squarer) or by modifying the trapezoid signal generator slightly to produce a waveform free of the continuous components. This is especially useful for circuits lacking an AC coupling.

It is worth mentioning that the general strategy has been customized to various cases of certain codec front-end chips. Some of them have been produced and are being tested in the factory; some of them are about to be prototyped on ASIC or FPGA (Field Programmable Gate Array) to perform their first real life tests, and some of them have shown very good simulation results and given a good tradeoff between the testing problem and the design margins conceptually. All of these can help us to find a proper BIST solution in the production test for the ADC/DAC pairs.

As noted in this dissertation, the loop structure allows proper verification. Nevertheless, combining the use of the BIST stimulus generator and that of the test equipment, the channels of the tester are only partially occupied. This aspect is very helpful in the production test, because as of today the number of chips that can be concurrently tested on ATEs is limited by the number of test channels. A higher level of parallelization would considerably speed up the testing time and, eventually, reduce the testing costs.

By implementation, the circuit under test and other functional components are treated

as the black boxes and only a keep/discard judgement has to be made. Extensions of the test strategy could be initially an application to other mixed signal chips and eventually a modification in the direction of diagnostic testing. This can be realized with the generation of a variety of test stimuli capable of identifying any single functional block and with an increase of the number of tests. This could also be useful for on-field system verifications.

Built-In Self-Test (BIST) design will continue to be an important topic in the area of production test. The techniques proposed in this dissertation are conceptual and therefore have the potential of being further improved or expanded to meet the future demands. Then the future work will be:

1) For the on-chip analog signal generator, the on-chip analog low pass filter is very important in the design. Although an off-chip analog LPF can be used, this will limit the BIST application.

2) The performance of the digital notch filter for evaluating the measurement response depends also on the settling time of the filter, which has the final influence on the total testing time. Future research on the same topic is recommended to further improve this work.

3) Due to time and cost limits, some BIST schemes were not fully implemented or only in concept. Further work can be pursued to implement the rest of the system.

4) Any silicon implementation of the improvement on the BIST components in the future is a worthwhile endeavor.

Appendix A

The Roadmap of the ATE Requirements

According to the reports of International Technology Roadmap for Semiconductors (ITRS) in 2001 and 2002 [4], we illustrate the requirements of the mixed-signal test equipment in Table A.1, which focuses on test instruments rather than specific IC device applications. Before going to the table, let's see some important areas of concern about the mixed-signal test equipments, which we quote directly from [4]:

- The analog/RF/microwave signal environment seriously complicates load board design and test methodology.

- Noise, crosstalk, signal mixing, load board design, and ATE software issues will dominate the test development process and schedule.

- Gigabit/second (2.5 to 10 GB/s) serial ports are being used for off-chip communication. These ports may be used on single ICs along with mixed-signal functions.

- Parallel test of all analog functions is needed to reduce test time, increase manufacturing cell throughput, and reduce test cost. This requires multiple instruments with fast parallel execution of DSP test algorithms (FFTs etc). Parallel test has been used for many years to test memory and high volume digital devices but not to a large enough extent on mixed-signal devices. Also, multiple analog functions on a single chip (such as dual, quad, octal, etc., for LAN ports) must be tested simultaneously.

- Better software tools that apply to more than one test equipment vendor are needed. Tools are required for digital and mixed-signal vector generation, circuit simulation of the device's analog circuitry along with the load board

and the test instruments, and rapid mixed-signal test program generation. Currently, mixed-signal test programs are manually generated; automatic test program generators are widely used for generating digital test.

In Table A.1, BW means Bandwidth, Fs means Sample rate, and MS/s means Mega samples/second. Moreover, AWG/Sin means arbitrary waveform generation/sine wave, SFDR is the spurious free dynamic range.

Table A.1: Mixed-signal test requirements [4]

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM(nm)	130	115	100	90	80	70	65
MPU / PITCH(nm)	150	130	107	90	80	70	65
PRINTED GATE LENGTH (nm)	90	75	65	53	45	40	35
PHYSICAL GATE LENGTH (nm)	65	53	45	37	32	28	25
Low Frequency Source and Digitizer							
BW (MHz)	15	22	30	40	50	60	60
Fs (MS/s)	5	7	10	13	16	20	20
Resolution (bits)	20-23	20-23	20-23	24	24	24	24
Noise floor (dB/RT Hz)	-160	-160	-160	-165	-165	-165	-165
High Frequency Waveform Source							
Level V (pk–pk)/ Accuracy (+/-)	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%
BW (MHz)	1600	2400	3200	4000	4800	6000	7000
Fs (MS/s)	3500	5000	7000	8500	10000	12000	15000
Resolution (bits) AWG/Sine	10/14	10/14	10/14	10/14	10/14	10/14	10/14
Noise floor (dB/RT Hz)	-145	-145	-150	-150	-155	-155	-155
High Frequency Waveform Digitizer							
Level V(pk–pk)/Accuracy (+/-)	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%	4/0.5%
BW (MHz)	2000	3000	4000	5200	6400	8000	92000
Fs (MS/s)	200	300	400	520	640	800	920
Resolution (bits)	12	12	12	12	14	14	14
Noise floor (dB/RT Hz)	-145	-145	-150	-150	-155	-155	-155
Time Measurement							
Jitter (ps)	3	2	2	1	1	1	1
Frequency (MHz)	660	1320	1320	1320	1640	2640	2640
Single shot time capability (ps)	100	75	75	75	50	50	50
RF/Microwave Instrumentation							

Source BW (GHz)/Accuracy (+/-dB)	10/0.2	14/0.2	14/0.2	18/0.2	18/0.1	18/0.1	18/0.1
Source phase noise low frequency, Close-In 1KHz (dBc/Hz)	130	136	136	136	136	136	136
Source phase noise high frequency Wideband 10MHz (dBc/Hz)	160	166	166	166	166	166	166
Receive BW (GHz)	10	14	14	14	18	18	18
Receive noise floor (dBm/Hz)	-160	-160	-160	-166	-166	-166	-166
Receive dynamic range SFDR (dBc)	110	130	140	140	140	160	160
Special Digital Capabilities							
D/A and A/D digital data rate (MB/s)	300	400	520	640	800	920	1040
Sample clock jitter (< ps RMS)	1.5	1.0	0.5	0.25	0.2	0.15	0.1

Here are the color meanings in the cells: white – manufacturable solutions exist, and are being optimized; yellow — manufacturable solutions are known; red – manufacturable solutions are still NOT known. And the definitions in Table A.1 are given as follows [4]:

- Low Frequency Source and Digitizer: this is the basic, minimum, instrument set of any mixed-signal tester. Telecommunications, advanced audio and wireless base band will drive these specifications. Differential inputs/outputs are needed.
- High Frequency Waveform Source: disk drive read channels (PRML) will drive sample rate and bandwidth. Local area network (LAN) devices will drive sample rate, bit resolution and amplitude accuracy. Differential outputs are needed.

- High Frequency Waveform Digitizer: an under-sampled (down conversion, track-and-hold, etc) bandwidth is shown. The sample rates and bit resolutions are for a direct conversion digitizer, which is usually preceded by the undersampler. PRML and LAN devices will drive digitizer specifications. Differential inputs are needed.

- Time Measurement: Phase Lock Loops (PLLs), which are increasingly being embedded in new designs, will require Jitter and Frequency measure-

ments. A specialized class of instruments will have to be developed to make these measurements efficiently and accurately.

- RF/Microwave Instrumentation: single chip RF/digital/baseband/audio devices will require RF instruments such as modulated carrier sources and low noise receivers or down converters.

- Special Digital Capabilities: for converter testing, the ability to source a digital word to a D/A and to capture a digital word from an A/D.

Current Analog/RF/Microwave testing methodologies require performance-based measurements (i.e., using external outside-the-chip instruments); therefore, instrument needs to reflect the increasing device performance predicted in the process and packaging technology roadmaps. The complexity of applications is also forcing specialized instrument designs focused on a particular device application. This complexity increases the number of instruments in a given test system, which increases cost and creates significant configuration-management issues for equipment that must be shared across multiple products. This trend of increasing instrument numbers, complexity, and performance is expected to continue but can not be allowed to drive up the cost.

Appendix B

The Design and Simulations Environments

B.1 Synopsys' COSSAP

COSSAP --COmmunication Systems Simulation and Analysis Package is a complete design environment that allows the engineer to construct complex hierarchical algorithmic functions. Its characteristics make COSSAP a tool useful for both theoretical studies and industrial simulations.

B.1.1 Evaluation of design tools

An evaluation of tools for digital signal processing designs should take into account [78] the level of abstraction, the definable data types, and the richness of the library, the optimization possibilities and the synthesis procedures.

Development tools can be most diverse but generally two main philosophies can be identified: those having a high-level of abstraction and those with a low-level of abstraction. The former are more general and closer to human thinking, whereas the latter are closer to hardware and therefore suitable for mapping to an ASIC, FPGA or DSP. An ideal design tool should cover both aspects, although almost incompatible. Many tool vendors have been trying to close the gap between concept and silicon realization, and COSSAP belongs to this attempt.

High level of abstraction tools lead to a behavioural design, where the focus is on defining and verifying the behaviour of a system or algorithm and only few decisions re-

garding implementation are taken. The key benefits of behavioural synthesis for DSP hardware design are:

- It allows rapid experimentation with a variety of approaches and to and new architectural optimizations that might not otherwise have been discovered.
- Change requests can be fast acknowledged.
- Debugging is faster, since it is easier to localize the malfunctioning block.
- Simulations are executed more quickly.

Many important semiconductor companies report reductions in design time thanks to the high-level tools. Lower-level designs, such as register-level VHDL description, reflect the pattern of the underlying physical hardware and as such are less intuitive for the human mind. This implies no at-a-glance understanding of complex structures and, consequently, all above-mentioned advantages of behavioral design are lost: debugging, modification and simulation are considerably slower, since all binary operations in the registers have to be described. If the technology is changed during project, or if a finished work has to be ported to a new architecture (for example should the previous technology become obsolete), the chip practically has to be redesigned. Furthermore, the fact that the designer must promptly specify the architectural-level means that he is not free to experiment with a wide range of design options. Such experimentation is crucial and often yields significant improvements in terms of design speed, cost, or power consumption.

It would seem that high-level tools provide the optimal design environment; on the other hand, at a certain point it is necessary to descend the ladder of abstraction to define the hardware architecture. This transition can be performed manually by the engineer or automatically (with more or less efficiency) by the design tool, which generates either VHDL or Verilog code to be used with logic synthesis tools. It can be seen that the main drawback of the behavioral approach is the fact that, to obtain good results, the designer must supervise and direct the “automatic" procedures very closely.

One approach used by block-diagram tools for generating hardware architecture from a behavioral circuit model is behavioral synthesis, supported also by Synopsys' COSSAP. This requires that general directives be provided to the tools, specifying how certain parts should (or should not) be implemented. The behavioral synthesis tools then generate hardware architectures described at register-transfer level (RTL), leaving it to

compatible lower-level logic synthesis tools to create a gate-level implementation. The idea behind behavioral synthesis is to maintain block-diagrams while supporting hardware development as well. Many of the lower-level blocks (e.g. adders) are provided, for instance, with an optimized VHDL code. Of course this is not the case with very high-level (e.g. transmitters) or purely simulation (e.g. Gaussian channel) models. For user-designed models the VHDL generator is provided which, as mentioned above, produces behavioral code. In COSSAP this has to be optimized by hand for the specific application.

B.1.2 Tool description

B.1.2.1 Blocks

A block is in COSSAP a function that reads x inputs and produces y outputs. Extensive built-in libraries of digital signal processing comprehend many primitive blocks. By placing several of these blocks in the editor and establishing their interconnections, a schematic can be intuitively realized.

The libraries contain floating point and fixed-point models. It is practical, for example, to experiment first with a floating point model to discover the optimal algorithm, as an alternative to software simulations with, e.g. MATLAB, and then to develop the corresponding bit-true implementations, systematically moving from the simpler to the more complex. New blocks can be built by writing directly the corresponding function in C or VHDL language or by creating a new schematic containing, along with primitive blocks, also input and output ports: this will be a hierarchical model. Either model is then compiled and added to a user-defined library. This way the original libraries can be enriched with user-designed primitive or composite models, maintaining the design flow hierarchical and easy to follow, a valuable advantage with more complex circuits comprising of several macro cells.

B.1.2.2 Parameters

Each block is provided with a set of parameters to control its properties during design. These parameters need to be configured, a procedure which can be done in two ways:

either by setting them to a fixed value, or by converting them to variables to be defined at the moment of simulation. Once again, the design can be kept at a higher level of abstraction longer, where critical decisions can be taken more easily. An annoying aspect of COSSAP is that it does not support the fractional arithmetic format commonly used on digital signal processors and in filter banks, but only integers. This limitation can be easily worked around by tracking the positions of the binary point, but it is an unnecessary burden.

B.1.2.3 Simulations

A schematic circuit is readied for simulation with a data stream-driven simulator. A particularity of COSSAP is that the simulation flow is data-driven instead of clock-driven, because an instance is activated only when all necessary stimuli are present at its input ports. The advantage is that multi-rate and asynchronous systems are readily represented and simulated without the need of scheduling the different clocks. The drawbacks are that the clock has to be simulated essentially with counters to enable signals and interpolators/decimators which increase/reduce the rate at different nodes.

An interesting aspect is that the simulator can be controlled concurrently, enabling interactive debugging and verification. There are practical options, for example, positioning monitors on wanted nodes and running a simulation one step at a time. Datasets obtained as a result of a simulation can be viewed with a graphing tool and further processed with a practical built-in calculator, comprising advanced operations such as FFT, or alternatively they can be exported in one of the many available formats for processing with other mathematical tools (e.g. MATLAB). Another practical feature is co-simulation. For example, a model may be realized in MATLAB and then imported as a COSSAP block and inserted in the libraries. During simulations, MATLAB will be called to run the particular associated routine.

B.1.2.4 Hardware implementations

COSSAP is not only a system-level design tool and simulator; it also tries to bridge the gap between algorithm and implementation. A complex digital signal processing design can, in principle, be taken through from concept to silicon.

After verifying the system through simulation, a netlist is generated, which can be fed to a VHDL code generator. COSSAP generates behavioural code, which describes the design as a sequence of operations to be performed rather than as a set of discrete hardware structures. This description is suitable for both synthesis and simulation. The project is not only more easily understood at this higher level, but also more flexible to modifications even late in the design cycle, resulting in a considerable design time reduction compared to hand-written implementation-oriented (RTL) code.

Furthermore, instruction sets for many leading DSP vendors can be automatically generated. Advantages of COSSAP recognized by their users are:

- Shortening of the chronical distance between system engineers and ASIC designers.
- Fast simulations, thanks to the absence of clock distribution and to the higher description level.
- Straightforward project re-use and porting to different technologies.

B.2 ModelSim

ModelSim is produced by Mentor Graphic for the simulation for VHDL or Verilog packages. And it is also the world's most popular and widely used VHDL and mixed-VHDL/Verilog simulator. ModelSim products are uniquely architected using technology such as Optimized Direct Compile for faster compile times and simulation performance, Single Kernel Simulation (SKS) and Tcl/Tk for greater levels of openness and faster debugging. The key benefits of the ModelSim are:

- Fastest compilation and competitive simulation performance with Direct Compile architecture.
- Seamless mixing of VHDL and Verilog with Single Kernel Simulation.
- Simplified portability and library maintenance made possible with machine- and simulator-version independence.

- Protected use and distribution of intellectual property guaranteed with compiled machine-independent object code.

- Fast, comprehensive debugging with an easy-to-use, full-featured graphical user interface.

- Easy customization enabled by Tcl/Tk.

- Complete standard support for VHDL and Verilog.

- Industry's broadest ASIC and FPGA vendor library support and integrated, third-party tool choices

More detailed information about ModelSim is available in the website of Mentor Graphic: https://www.mentor.com

B.3 Design compiler

Design Compiler family is a set of logic synthesis tools that automatically create an gate-level design based upon an IC design specification and constraints. It is produced by Synopsys. The product family accommodates a wide range of design styles -- HDL, schematic, netlist. As the logic synthesis tool, it includes several performance-oriented features, which include support for design styles including latches and complex synchronous clocking schemes. It also incorporates a sophisticated in-place optimization technique that enables to bring design information back within specification, post-layout, without changing the netlist.

DC Expert *Plus*(TM) is Synopsys' premier synthesis product, which enables to implement a design-for-test (DFT) methodology with a synthesis-based design flow. It can operate on modules starting from HDL, or an imported netlist, or reuse blocks with existing scan. It can synthesize a design from HDL directly to optimized, testable gates (1-pass scan synthesis), or insert and route scan chains into an existing design (constraint-optimized scan insertion). The key benefits of Design Compiler are:

- Fastest route to silicon. Increases designer productivity through automatic gate-level implementation.

- Proven solution. World's most widely used logic synthesis product family-proven in 50,000-plus designs with more than 60 semiconductor vendors.

- Most complete synthesis solution. High-level synthesis capabilities embedded timing analyzer, links to test and layout, and solutions for ASICs and FPGAs.

More detailed information about Design Compiler is available in the website of Synopsys: http://www.synopsys.com/

Appendix C

Glossary of Abbreviations

ABSC	Analog Boundary Scan Cell
ADC	Analog-to-Digital Converter
ASMD	Application-Specific Multirate DSP
ATDI	Analog Test Data Input
ATDO	Analog Test Data Output
ATE	Automatic Testing Equipment
BIBO	Bounded Input Bounded Output
BIST	Built-In Self-Test
BPF	Band Pass Filter
CAD	Computer Aided Design
CMPR	Common Mode Rejection Ratio
CORDIC	Coordinate Rotation Digital Computer
CSD	Canonical Signed Digit
CUT	Circuit under Test
ENOB	Effective Number of Bits
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transforms
DNL	Differential Nonlinearity
DSM	Delta-Sigma Modulator
DSP	Digital Signal Processor
FIR	Finite Impulse Response
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Arrays
IC	Integrated Circuit
IFA	Inductive Fault Analysis
IIR	Infinite Impulse Response
INL	Integral Nonlinearity

LSB	Least Significant Bit
LUT	Look-Up Tables
LPF	Low Pass Filter
LFSR	Linear-Feedback Shift Register
MSB	Maximum Significant Bit
MMI	Man Machine Interface
PLL	Phase Lock Loop
PSSR	Power Supply Rejection Ratio
PDM	Pulse Density Modulated
PRBS	Pseudo-Random Bit Sequence
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
VHDL	VLSI Hardware Description Language
VLSI	Very Large Scale Integration
WDF	Wave Digital Filter

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